Dampers for Main Injector/RR

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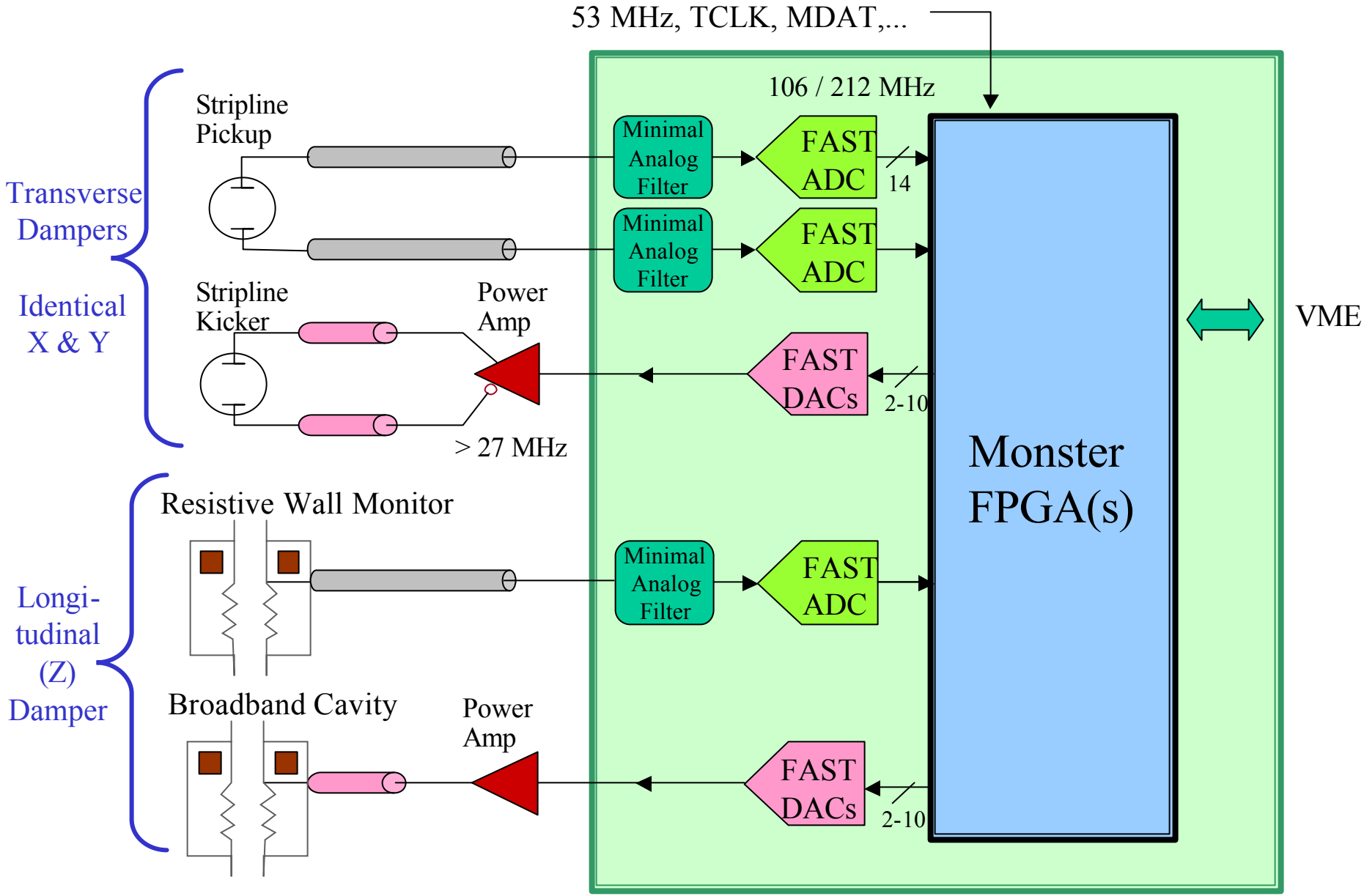
Warren Schappert, Dave Wildman,
Bill Ashmanskas (emeritus)

May ‘03

MI/RR Damper

- Digital Damper Design
- Hardware Status
- Beam Results
- ACNET/Control Interface
- Other Applications

All-Coordinate Digital Damper



Wide Variety of Beam Dampers Required in MI & Recycler

1) Transverse (X,Y) and Longitudinal

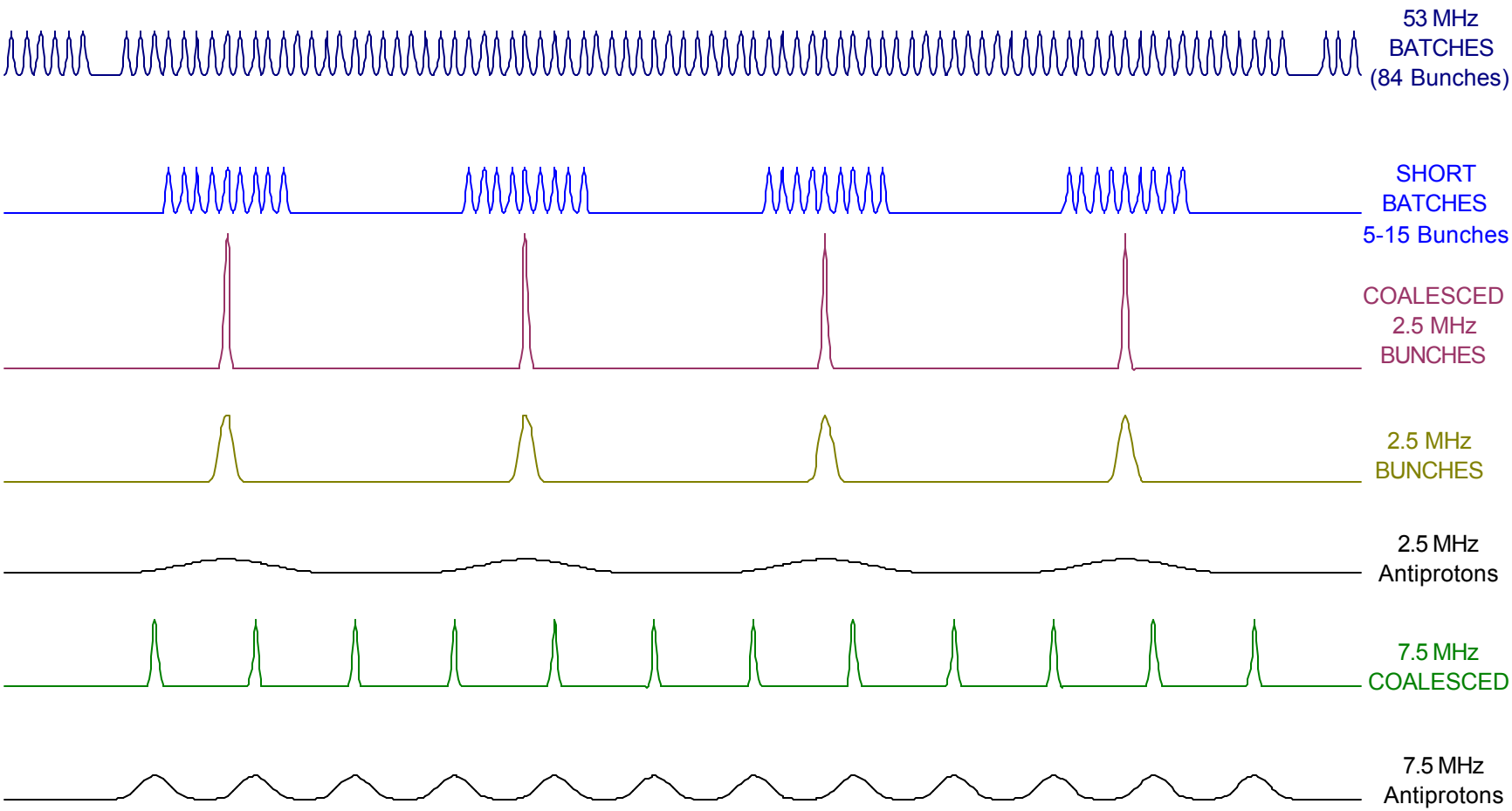
2) 53 MHz, 2.5 MHz, 7.5 MHz, and DC Beam

3) Single Bunches, Full Batches, Short Batches

4) Injection, Ramping, and Stored Beam

5) Pbar and Proton Directions (✍ different timing)

Beam Bunch Structures in Fermilab Main Injector



... plus unbunched DC Beam in Recycler...

Damper Operating Modes

	Booster		Main Inj.		Recycler		Tevatron	
	Pbar	P	Pbar	P	Pbar	P	Pbar	P
53 MHz Full Batches		X		X		C		
53 MHz Short Batches			X	X				
53 MHz Coalesced Bunch			X	X			X	X
2.5 MHz Batch (4)			X	C	X	C		
7.5 MHz Batch (12)			X	C				
DC Beam					X	C		

X = Operation **C** = Commissioning & Tuneup

Damper Priorities in Main Injector & Recycler

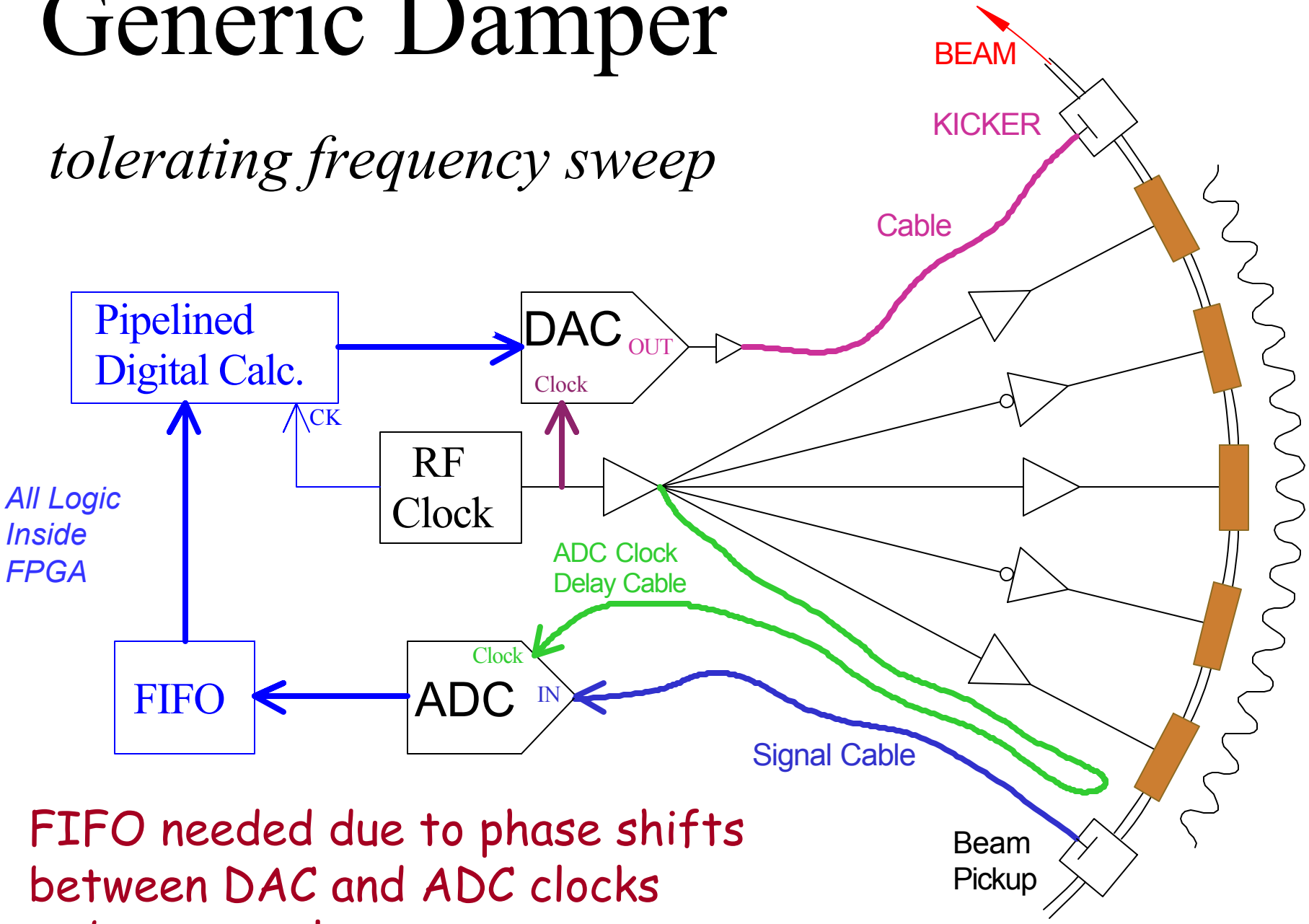
1. Main Injector Longitudinal Dampers
2. Main Injector Transverse Dampers
3. Recycler Transverse Injection Dampers
4. Recycler Longitudinal Dampers
5. Recycler Broadband (DC Beam) Dampers

Advantages of Digital Filters

- Digital filters more reproducible (=>spares!)
- Inputs and Outputs clearly defined (& stored!)
  - filters can be developed & debugged offline
- Digital filter can also operate at multiple lower frequencies ...simultaneously if desired.
  - ? MI will not be blind for 2.5 and 7.5 MHz Beam
- Re-use Standard hardware with new FPGA code
  - or same code with different filter coefficients

Generic Damper

tolerating frequency sweep



FIFO needed due to phase shifts between DAC and ADC clocks as beam accelerates

What ADC Clock Speed is needed?

- ~53 MHz Bandwidth limited signal, sampled by 106 MHz ADC, measures either *in-phase* (cosine) or *quadrature* (sine) component
  - but not both ==> ADC clock phasing matters!

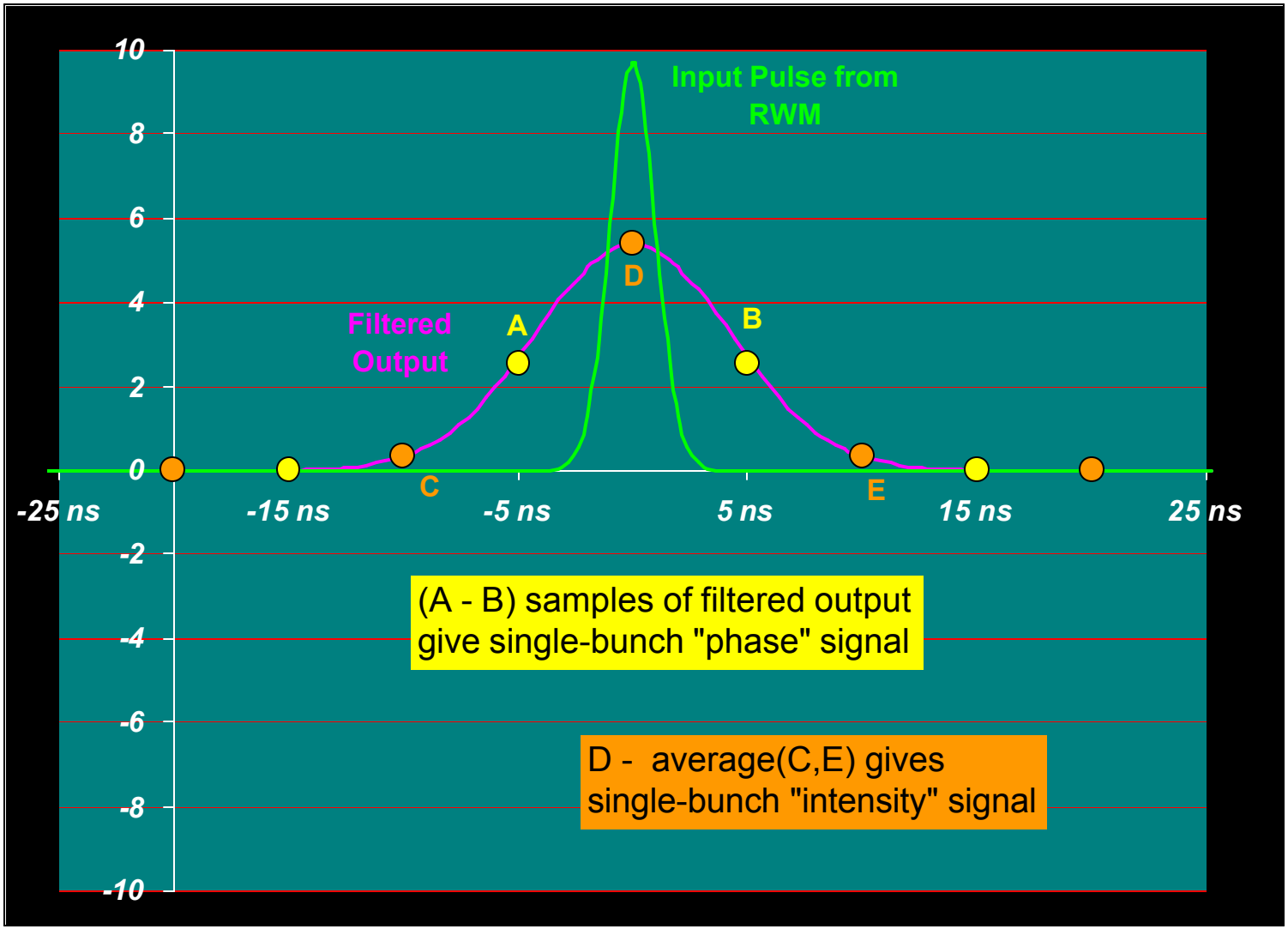
- 212 MHz sampling measures both *in-phase* and *quadrature* components. *Phasing is not critical* to determine vector magnitude.

- 212 MHz ✍built in phase measurement

Bandwidth Limit Signal

- Raw signal has high-frequency components which can cause signal to be missed by ADC
  - "Aliasing"
- Bandwidth limited signal (to ~50 MHz) so cannot be missed by 212 MHz ADC
- Eliminate low-frequency ripple, baseline shifts, etc. with Transformer or AC coupling
  - Digital Filtering can provide additional rejection

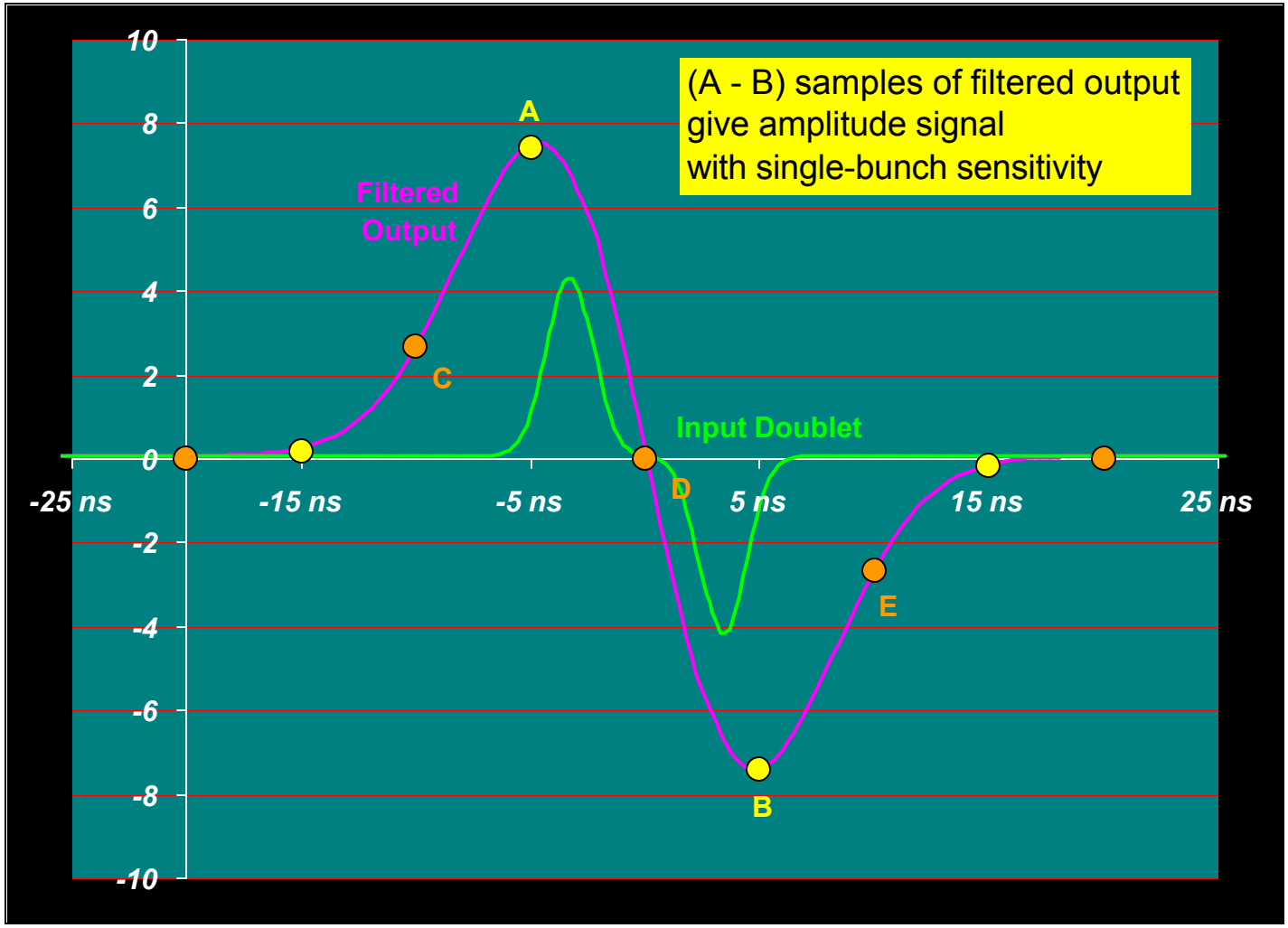
212 MHz Sampling of RWM Pulse



Low-pass Filter Spreads signal +/-5ns in time so it will not be missed by ADC

Reduces ADC Dynamic Range requirement, since spike does not have to be digitized

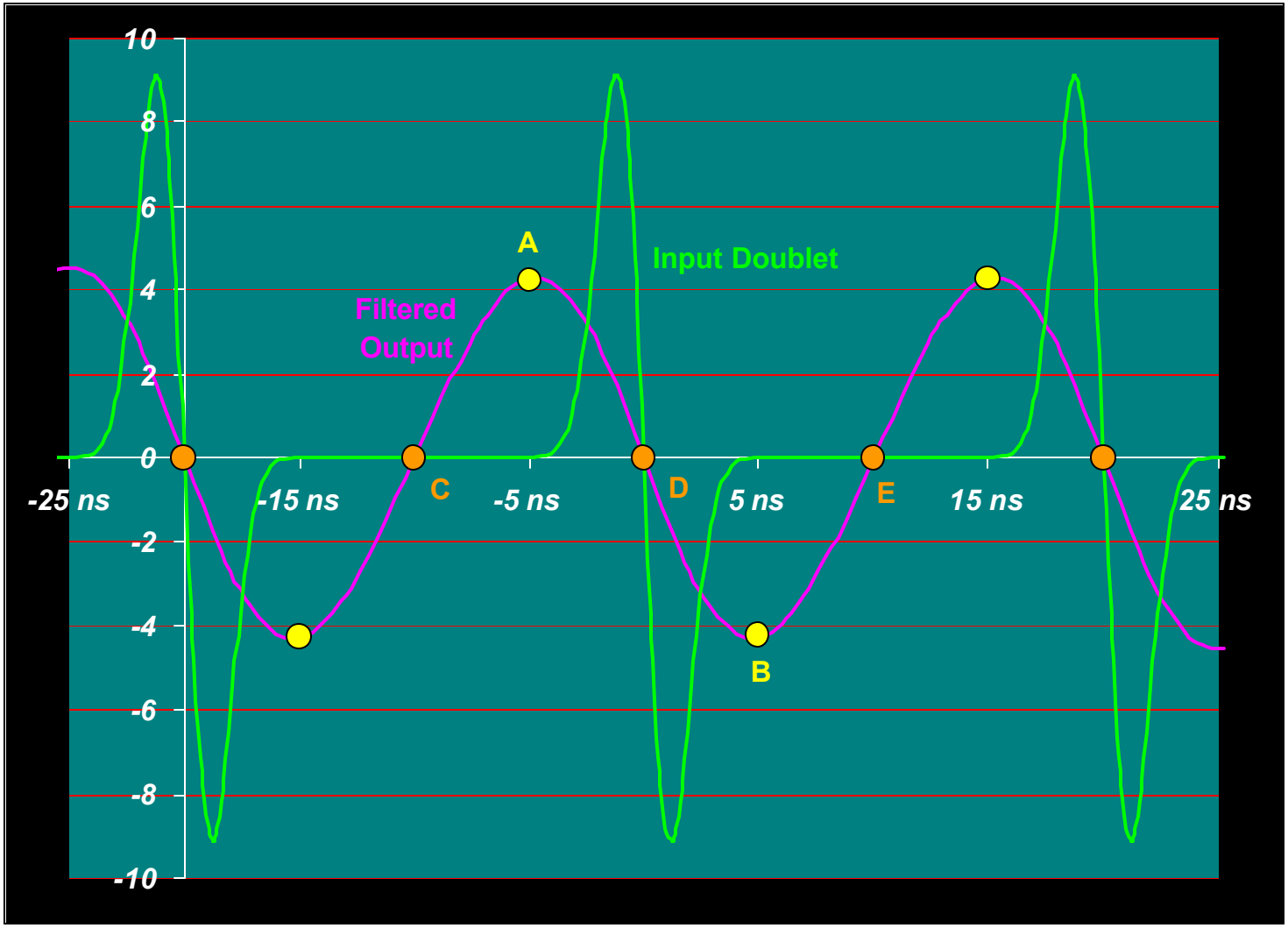
212 MHz Sampling of Stripline Signal



Filter Spreads signal +/-5ns in time so it will not be missed by ADC

Signal difference from points (A-B) has no first-order sensitivty to phase errors

Repetitive Waveform looks like simple sine wave, but contains bunch-by-bunch phase and amplitude



"A - B" gives bunch-by-bunch "in-phase" signal

"D - (C+E)/2" gives bunch-by-bunch "out-of-phase" or "quadrature" signal

Vector Sum sqrt(I**2 +Q**2) is insensitive to clock jitter

Echotek Card Used for Initial Dampers

ECHOTEK CORP.

EIGHT CHANNEL
ANALOG TO DIGITAL CONVERTER
~~WITH DIGITAL RECEIVER~~

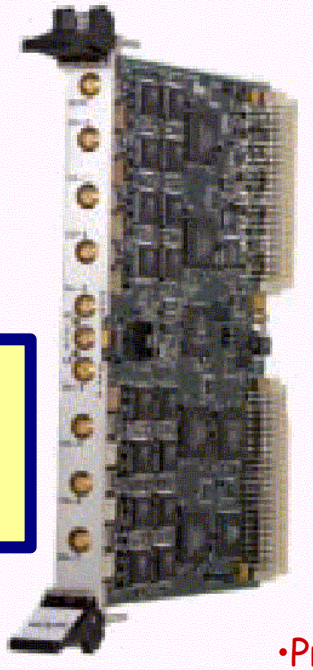
ECDR-814/X-AD

FEATURES

* 8 IF INPUTS
* SIMULTANEOUS SAMPLING
* EIGHT ANALOG TO DIGITAL CONVERTERS (ANALOG DEVICES AD6644, 14 BIT, 65 MSPS)
* SFDR > 90 dB FS
* HEADER INSERTION
* VME 64X, SINGLE SLOT
* RACE++ OUTPUT
* AVAILABLE AS A/D CONVERTER AS AN 8, 4, OR 2 CHANNEL MODULE
* VARIABLE GAIN (~ -10 TO +20 dB) OR LOW PASS FILTER

105 MSPS

AD6645

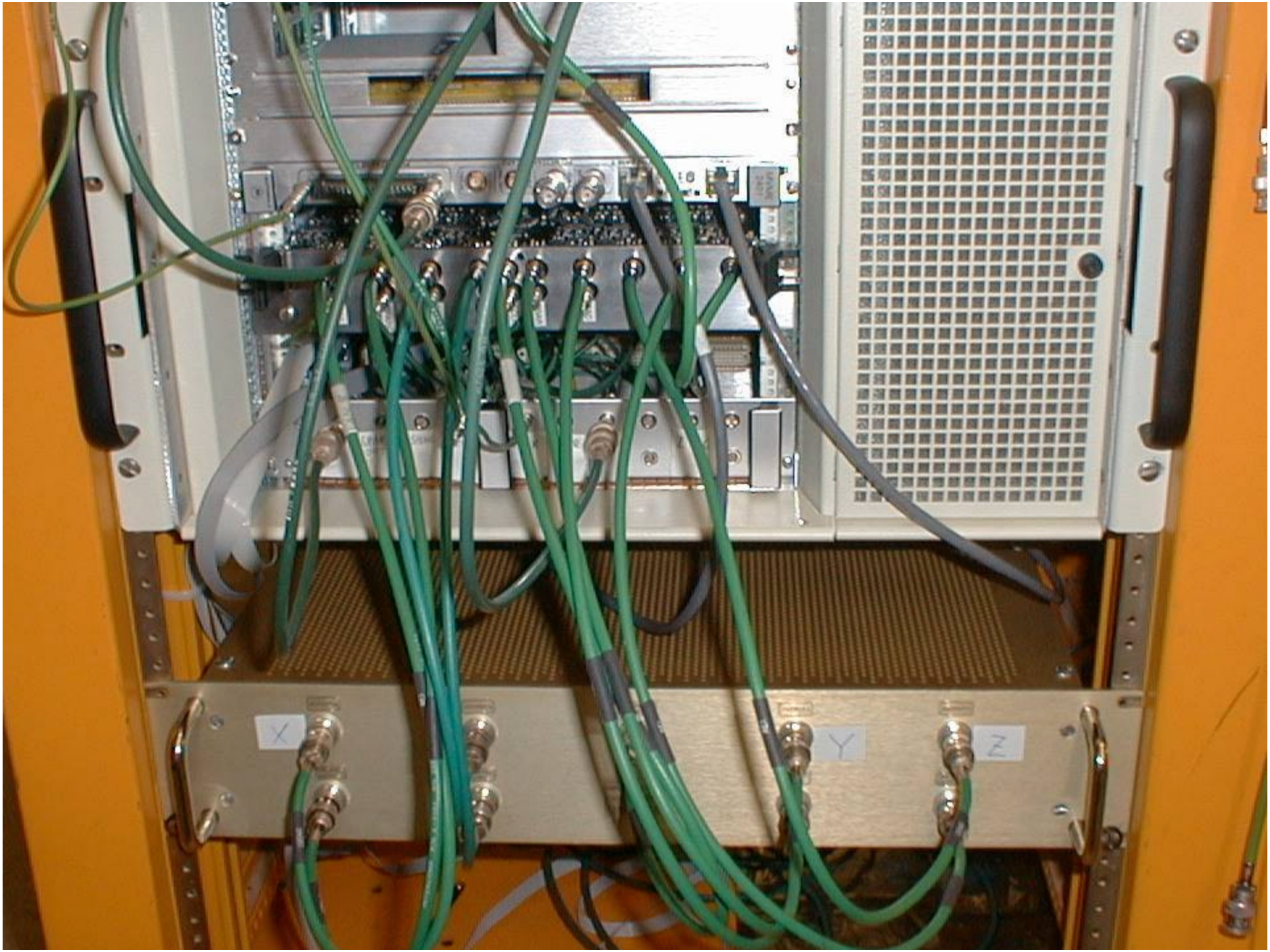


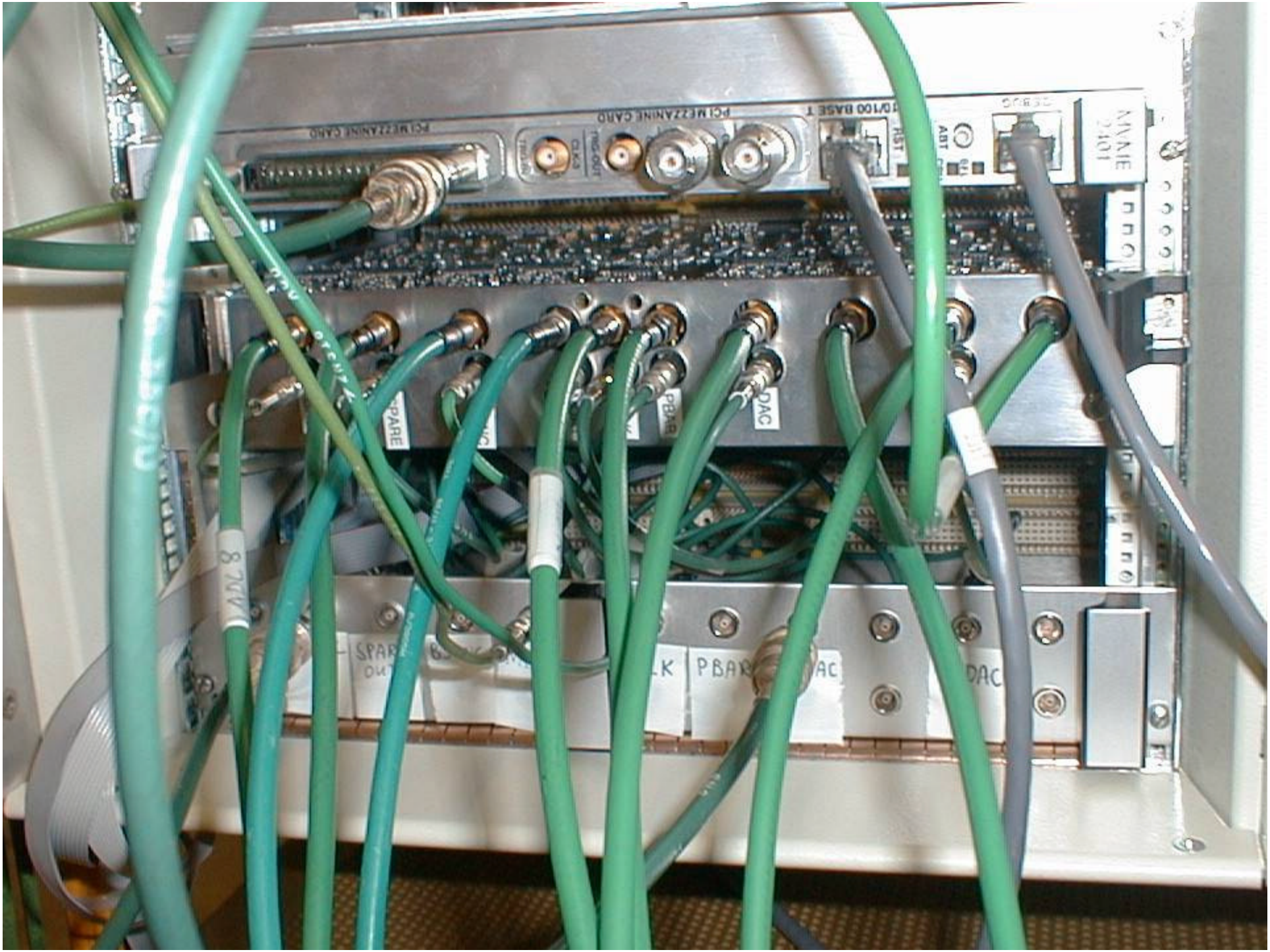
✍ 212 MHz DAC Daughter Card (S. Hansen/ PPD) due this week

•Prieto, Meyer et. al. evaluating 65MHz DDC for RR BPM upgrade
•Asmanskas, Foster, Schappert testing 105 MHz version for RR Dampers

Butchering the Echotek Board

- Scorched-Earth FPGA rewrite (GWF)
  - ~65 pages of firmware since Jan '03
- 212 MHz DAC Daughtercard
  - Sten Hansen & T. Wesson (PPD)
  - 3 channels for X,Y,Z
- 200 MHz Output FIR (W. Schappert, RFI)
  - Pre-emphasis compensation for analog outputs
  - Prototype for 424 MHz output on final board
- Input Buffer Amp/Splitter Box (Brian Fellenz,RFI)


X
Y
Z

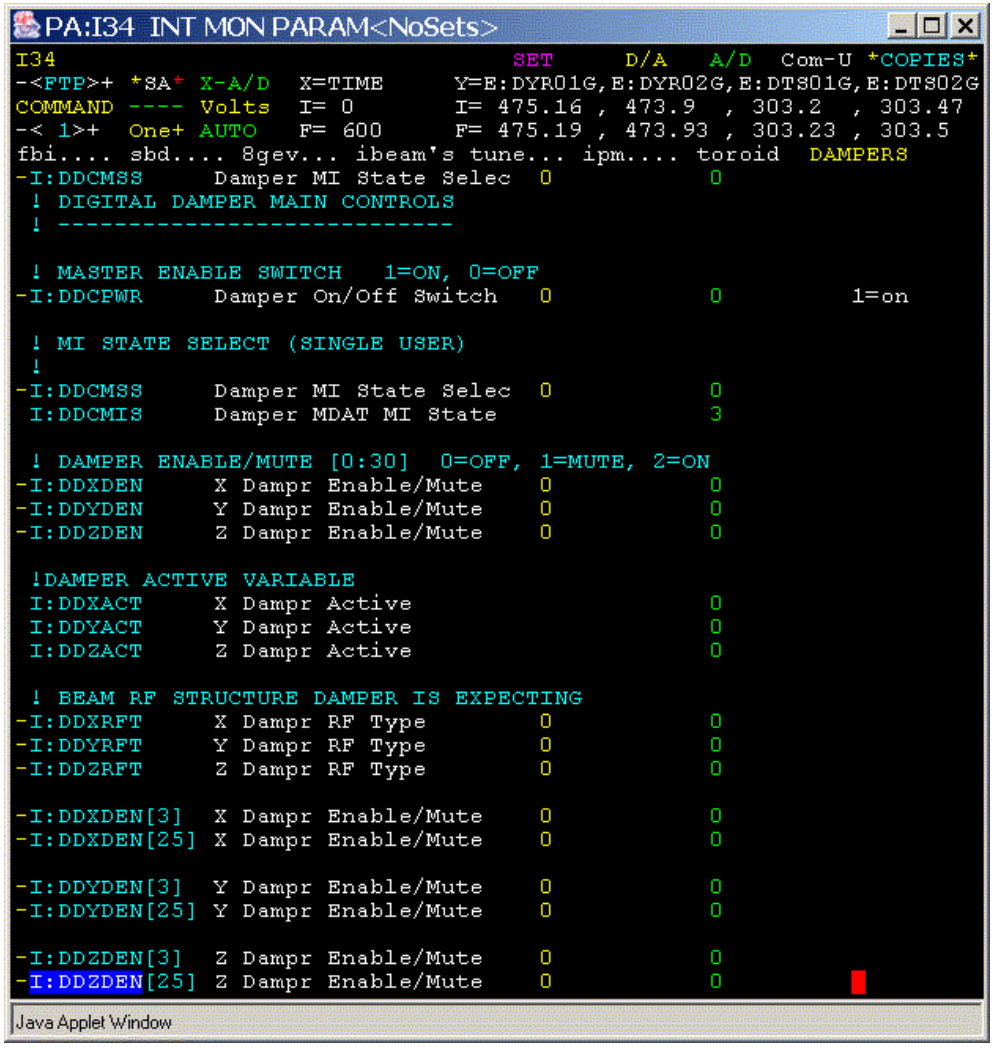

PCI MEZZANINE CARD
10/100 BASE T
ACT
LNK
MMIE
SLOT
PBARE
DAC
SPAR
PBAR
DAC


H602
V601
V601

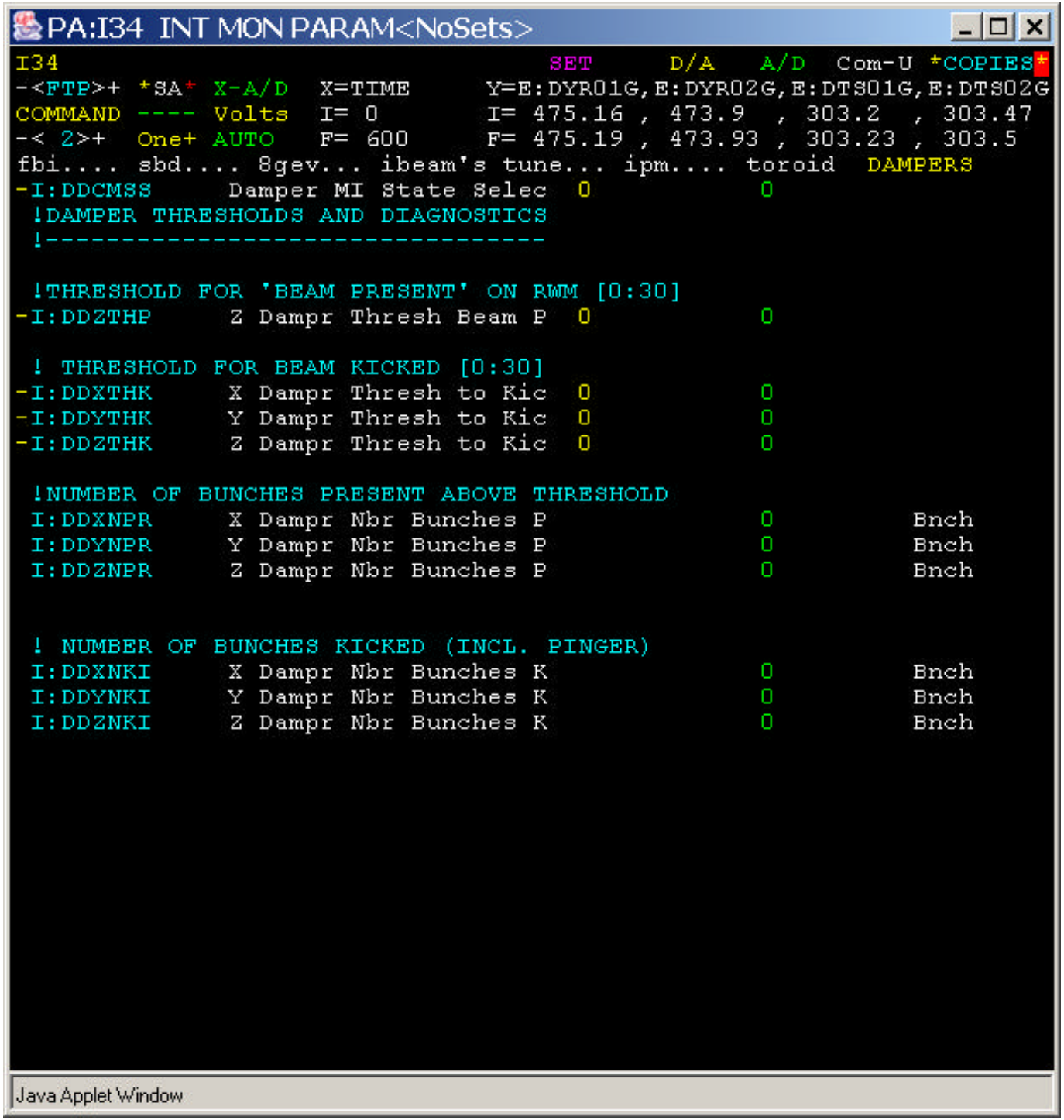
ACNET CONTROLS

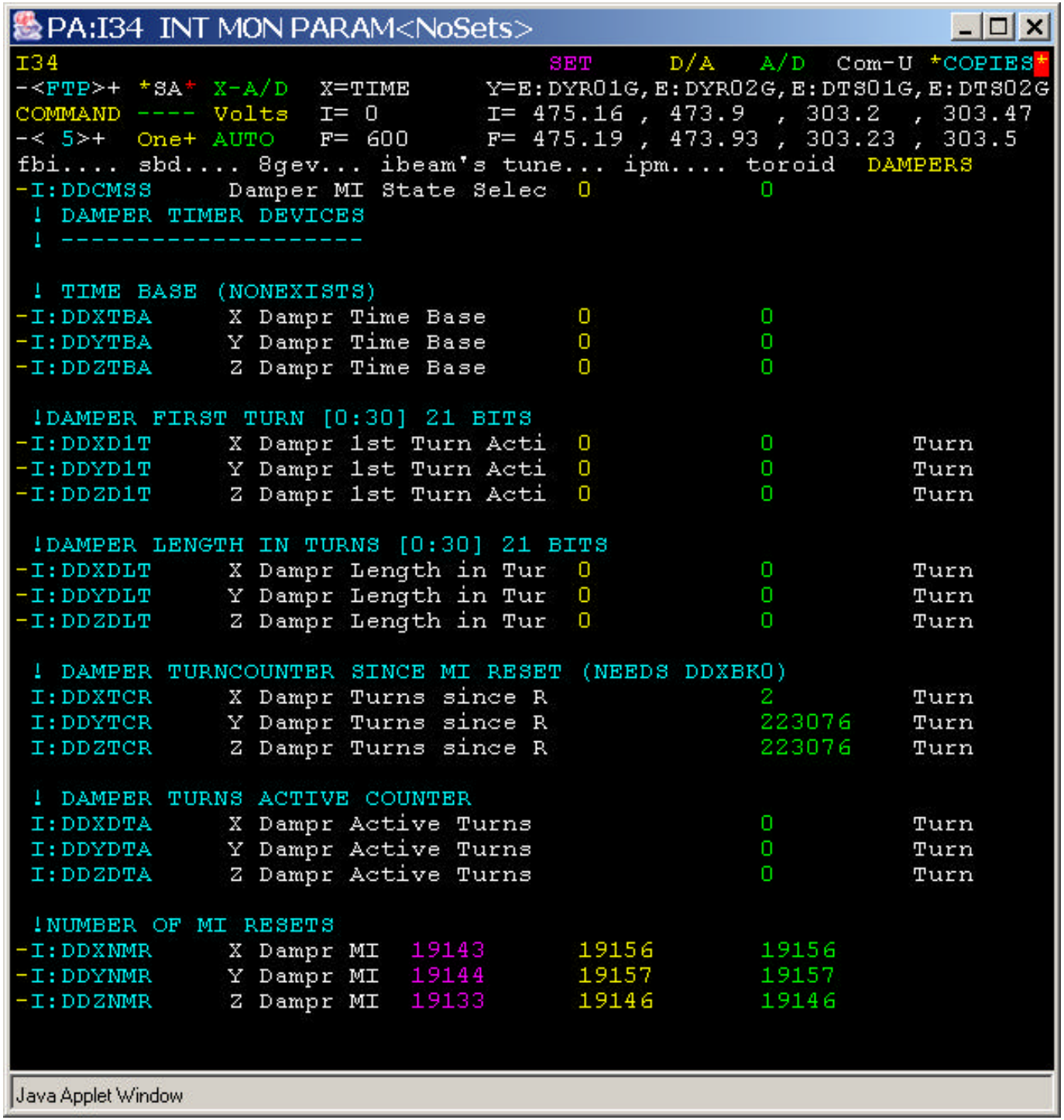
- Damper must behave differently for different bunches ✍ bunch-by-bunch RAM
  - Specifies Damper Gain, anti damp, noise injection, pinging, etc. on bunch-by-bunch basis.
- Damper must behave differently on different MI cycles
  - Each control register becomes an ACNET Array Device indexed by MI State
  - Register contents switch automatically when MI State changes *(D. Nicklaus)*

ACNET Control Devices (>250 total)



- Master control registers & diagnostics are typically single devices
- Configuration control registers are array devices indexed by MI State


PA:I34 INT MON PARAM<NoSets>
I34 SET D/A A/D Com-U *COPIES*
-<FTP>+ *SA* X-A/D X=TIME Y=E:DYR01G,E:DYR02G,E:DTS01G,E:DTS02G
COMMAND ---- Volts I= 0 I= 475.16 , 473.9 , 303.2 , 303.47
-< 2>+ One+ AUTO F= 600 F= 475.19 , 473.93 , 303.23 , 303.5
fbi.... sbd.... 8gev... ibeam's tune... ipm.... toroid DAMPERS
-I:DDCMSS Damper MI State Selec 0 0
!DAMPER THRESHOLDS AND DIAGNOSTICS
!----------
!THRESHOLD FOR 'BEAM PRESENT' ON RWM [0:30]
-I:DDZTHP Z Dampr Thresh Beam P 0 0
! THRESHOLD FOR BEAM KICKED [0:30]
-I:DDXTHK X Dampr Thresh to Kic 0 0
-I:DDYTHK Y Dampr Thresh to Kic 0 0
-I:DDZTHK Z Dampr Thresh to Kic 0 0
!NUMBER OF BUNCHES PRESENT ABOVE THRESHOLD
I:DDXNPR X Dampr Nbr Bunches P 0 Bnch
I:DDYNPR Y Dampr Nbr Bunches P 0 Bnch
I:DDZNPR Z Dampr Nbr Bunches P 0 Bnch
! NUMBER OF BUNCHES KICKED (INCL. PINGER)
I:DDXNKI X Dampr Nbr Bunches K 0 Bnch
I:DDYNKI Y Dampr Nbr Bunches K 0 Bnch
I:DDZNKI Z Dampr Nbr Bunches K 0 Bnch
Java Applet Window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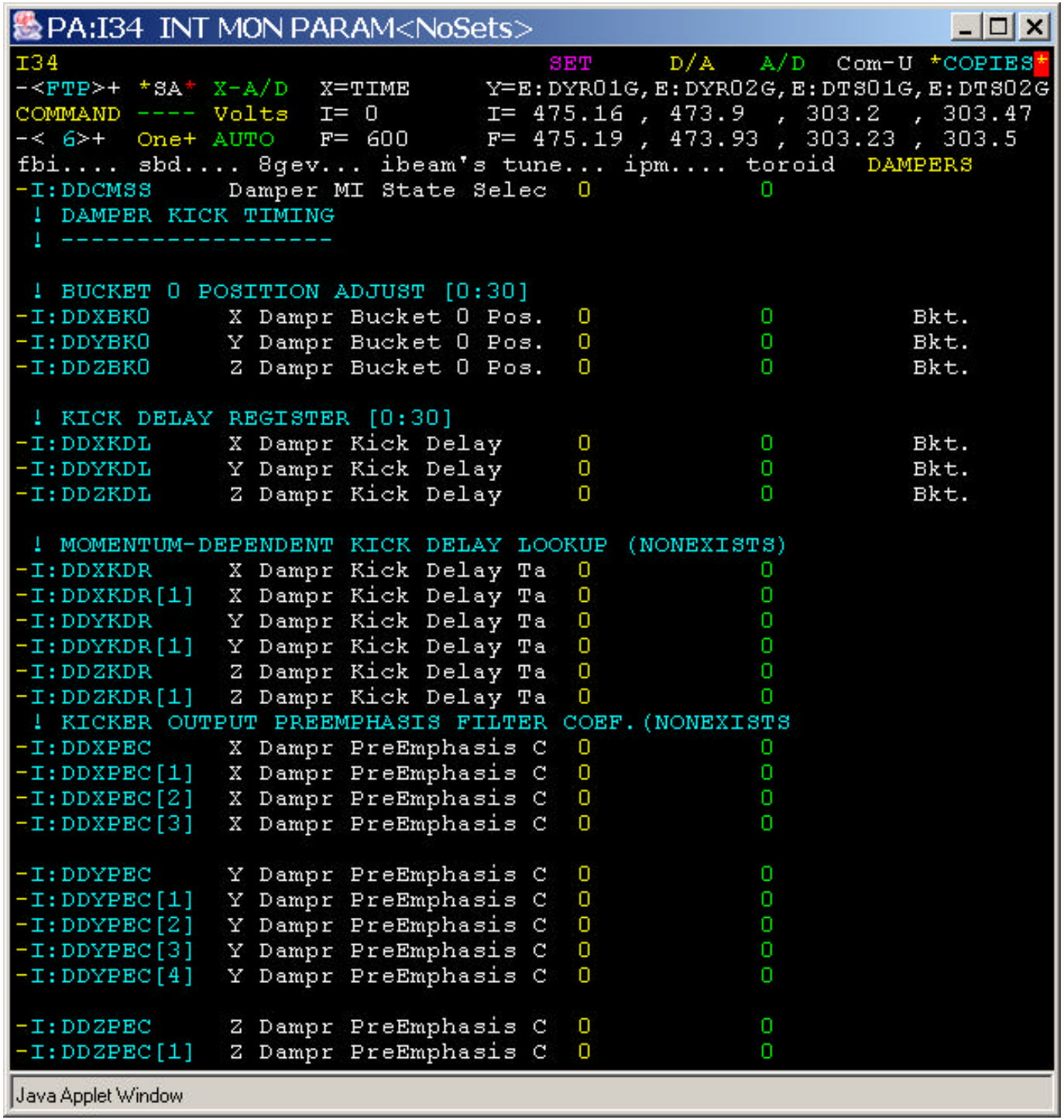
COMMAND ---- Volts I= 0 I= 475.16 , 473.9 , 303.2 , 303.47
-< 5>+ One+ AUTO F= 600 F= 475.19 , 473.93 , 303.23 , 303.5
fbi.... sbd.... 8gev... ibeam's tune... ipm.... toroid DAMPERS
-I:DDCMSS Damper MI State Selec 0 0
! DAMPER TIMER DEVICES
! --------------------
! TIME BASE (NONEXISTS)
-I:DDXTBA X Dampr Time Base 0 0
-I:DDYTBA Y Dampr Time Base 0 0
-I:DDZTBA Z Dampr Time Base 0 0
!DAMPER FIRST TURN [0:30] 21 BITS
-I:DDXD1T X Dampr 1st Turn Acti 0 0 Turn
-I:DDYD1T Y Dampr 1st Turn Acti 0 0 Turn
-I:DDZD1T Z Dampr 1st Turn Acti 0 0 Turn
!DAMPER LENGTH IN TURNS [0:30] 21 BITS
-I:DDXDLT X Dampr Length in Tur 0 0 Turn
-I:DDYDLT Y Dampr Length in Tur 0 0 Turn
-I:DDZDLT Z Dampr Length in Tur 0 0 Turn
! DAMPER TURNCOUNTER SINCE MI RESET (NEEDS DDXBK0)
I:DDXTCR X Dampr Turns since R 2 Turn
I:DDYTCR Y Dampr Turns since R 223076 Turn
I:DDZTCR Z Dampr Turns since R 223076 Turn
! DAMPER TURNS ACTIVE COUNTER
I:DDXDTA X Dampr Active Turns 0 Turn
I:DDYDTA Y Dampr Active Turns 0 Turn
I:DDZDTA Z Dampr Active Turns 0 Turn
!NUMBER OF MI RESETS
-I:DDXNMR X Dampr MI 19143 19156 19156
-I:DDYNMR Y Dampr MI 19144 19157 19157
-I:DDZNMR Z Dampr MI 19133 19146 19146
Java Applet Window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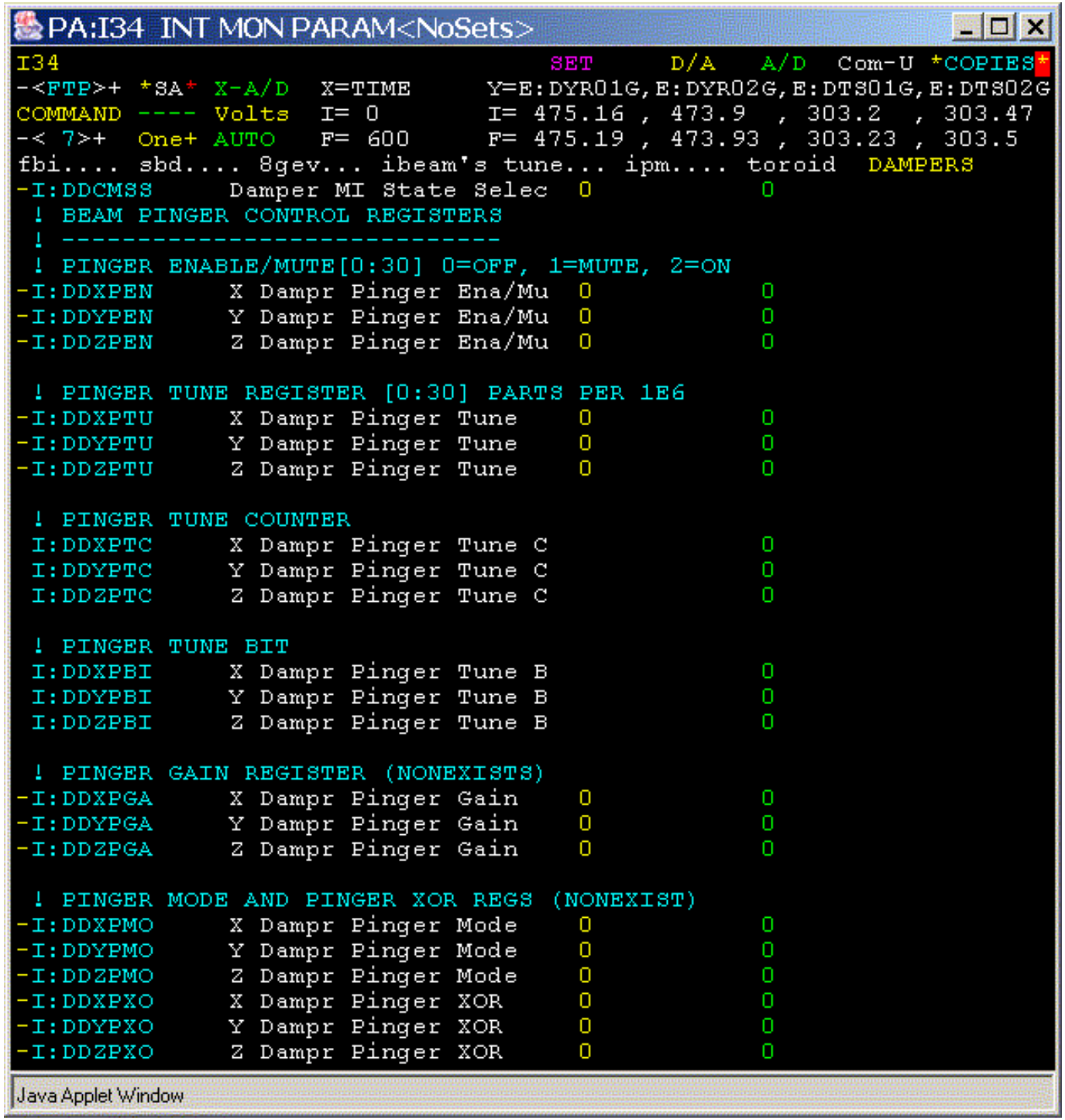
-< 6>+ One+ AUTO F= 600 F= 475.19 , 473.93 , 303.23 , 303.5
fbi.... sbd.... 8gev... ibeam's tune... ipm.... toroid DAMPERS
-I:DDCMSS Damper MI State Selec 0 0
! DAMPER KICK TIMING
! ----------
! BUCKET 0 POSITION ADJUST [0:30]
-I:DDXBK0 X Dampr Bucket 0 Pos. 0 0 Bkt.
-I:DDYBK0 Y Dampr Bucket 0 Pos. 0 0 Bkt.
-I:DDZBK0 Z Dampr Bucket 0 Pos. 0 0 Bkt.
! KICK DELAY REGISTER [0:30]
-I:DDXKDL X Dampr Kick Delay 0 0 Bkt.
-I:DDYKDL Y Dampr Kick Delay 0 0 Bkt.
-I:DDZKDL Z Dampr Kick Delay 0 0 Bkt.
! MOMENTUM-DEPENDENT KICK DELAY LOOKUP (NONEXISTS)
-I:DDXKDR X Dampr Kick Delay Ta 0 0
-I:DDXKDR[1] X Dampr Kick Delay Ta 0 0
-I:DDYKDR Y Dampr Kick Delay Ta 0 0
-I:DDYKDR[1] Y Dampr Kick Delay Ta 0 0
-I:DDZKDR Z Dampr Kick Delay Ta 0 0
-I:DDZKDR[1] Z Dampr Kick Delay Ta 0 0
! KICKER OUTPUT PREEMPHASIS FILTER COEF.(NONEXISTS
-I:DDXPEC X Dampr PreEmphasis C 0 0
-I:DDXPEC[1] X Dampr PreEmphasis C 0 0
-I:DDXPEC[2] X Dampr PreEmphasis C 0 0
-I:DDXPEC[3] X Dampr PreEmphasis C 0 0
-I:DDYPEC Y Dampr PreEmphasis C 0 0
-I:DDYPEC[1] Y Dampr PreEmphasis C 0 0
-I:DDYPEC[2] Y Dampr PreEmphasis C 0 0
-I:DDYPEC[3] Y Dampr PreEmphasis C 0 0
-I:DDYPEC[4] Y Dampr PreEmphasis C 0 0
-I:DDZPEC Z Dampr PreEmphasis C 0 0
-I:DDZPEC[1] Z Dampr PreEmphasis C 0 0
Java Applet Window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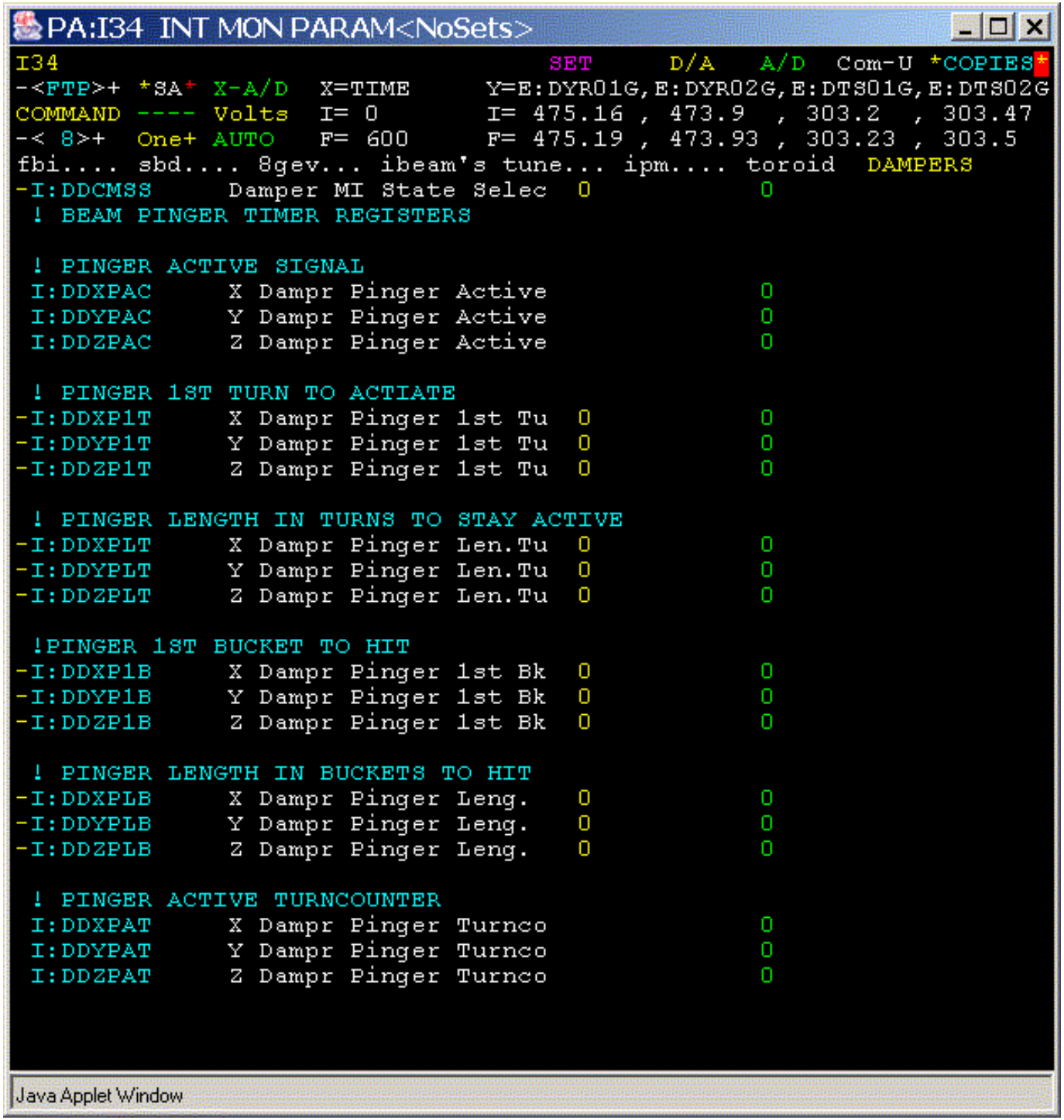
-< 7>+ One+ AUTO F= 600 F= 475.19 , 473.93 , 303.23 , 303.5
fbi.... sbd.... 8gev... ibeam's tune... ipm.... toroid DAMPERS
-I:DDCMSS Damper MI State Selec 0 0
! BEAM PINGER CONTROL REGISTERS
! ----------
! PINGER ENABLE/MUTE[0:30] 0=OFF, 1=MUTE, 2=ON
-I:DDXPEN X Dampr Pinger Ena/Mu 0 0
-I:DDYPEN Y Dampr Pinger Ena/Mu 0 0
-I:DDZPEN Z Dampr Pinger Ena/Mu 0 0
! PINGER TUNE REGISTER [0:30] PARTS PER 1E6
-I:DDXPTU X Dampr Pinger Tune 0 0
-I:DDYPTU Y Dampr Pinger Tune 0 0
-I:DDZPTU Z Dampr Pinger Tune 0 0
! PINGER TUNE COUNTER
I:DDXPTC X Dampr Pinger Tune C 0
I:DDYPTC Y Dampr Pinger Tune C 0
I:DDZPTC Z Dampr Pinger Tune C 0
! PINGER TUNE BIT
I:DDXPBI X Dampr Pinger Tune B 0
I:DDYPBI Y Dampr Pinger Tune B 0
I:DDZPBI Z Dampr Pinger Tune B 0
! PINGER GAIN REGISTER (NONEXISTS)
-I:DDXPGA X Dampr Pinger Gain 0 0
-I:DDYPGA Y Dampr Pinger Gain 0 0
-I:DDZPGA Z Dampr Pinger Gain 0 0
! PINGER MODE AND PINGER XOR REGS (NONEXIST)
-I:DDXPMO X Dampr Pinger Mode 0 0
-I:DDYPMO Y Dampr Pinger Mode 0 0
-I:DDZPMO Z Dampr Pinger Mode 0 0
-I:DDXPXO X Dampr Pinger XOR 0 0
-I:DDYPXO Y Dampr Pinger XOR 0 0
-I:DDZPXO Z Dampr Pinger XOR 0 0
Java Applet Window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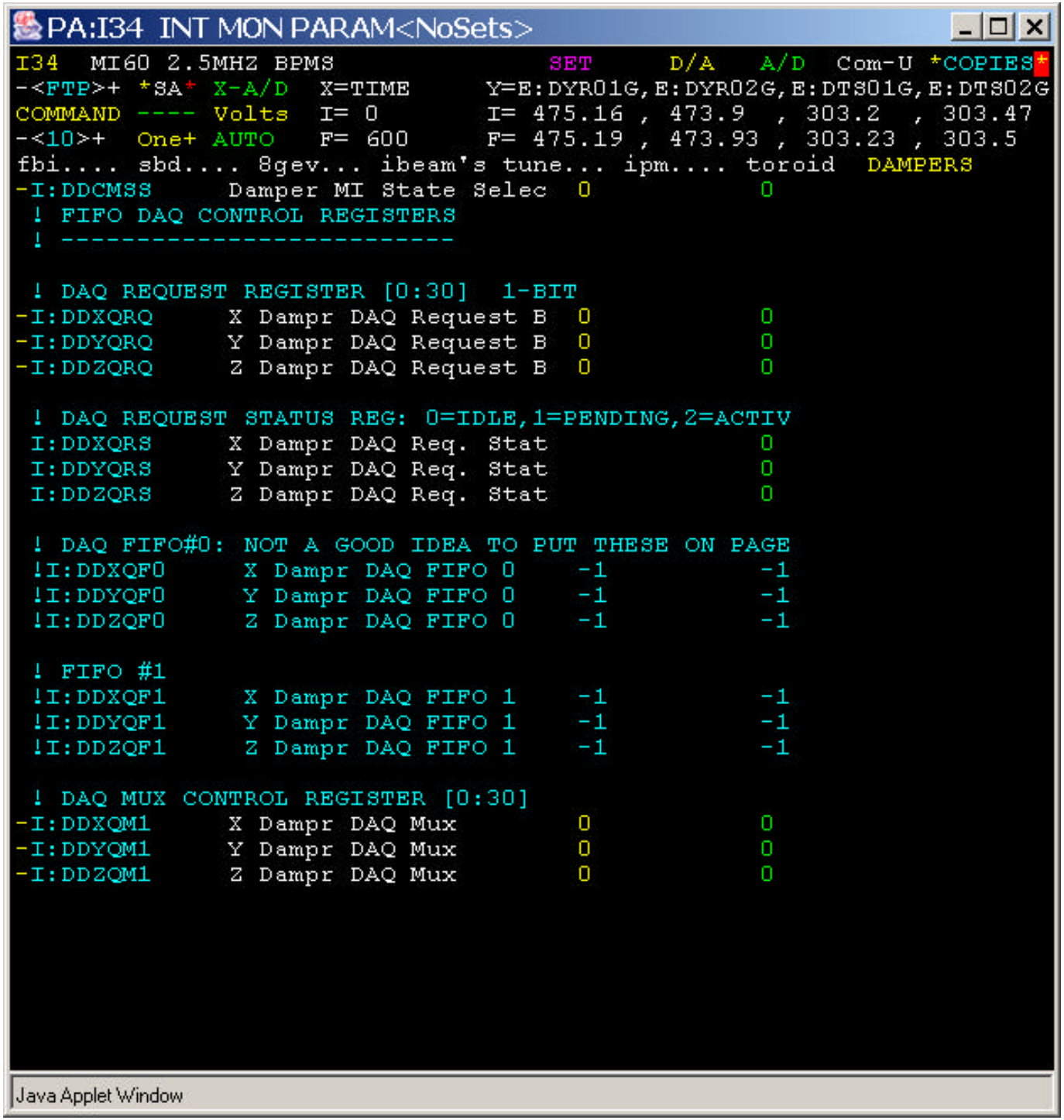
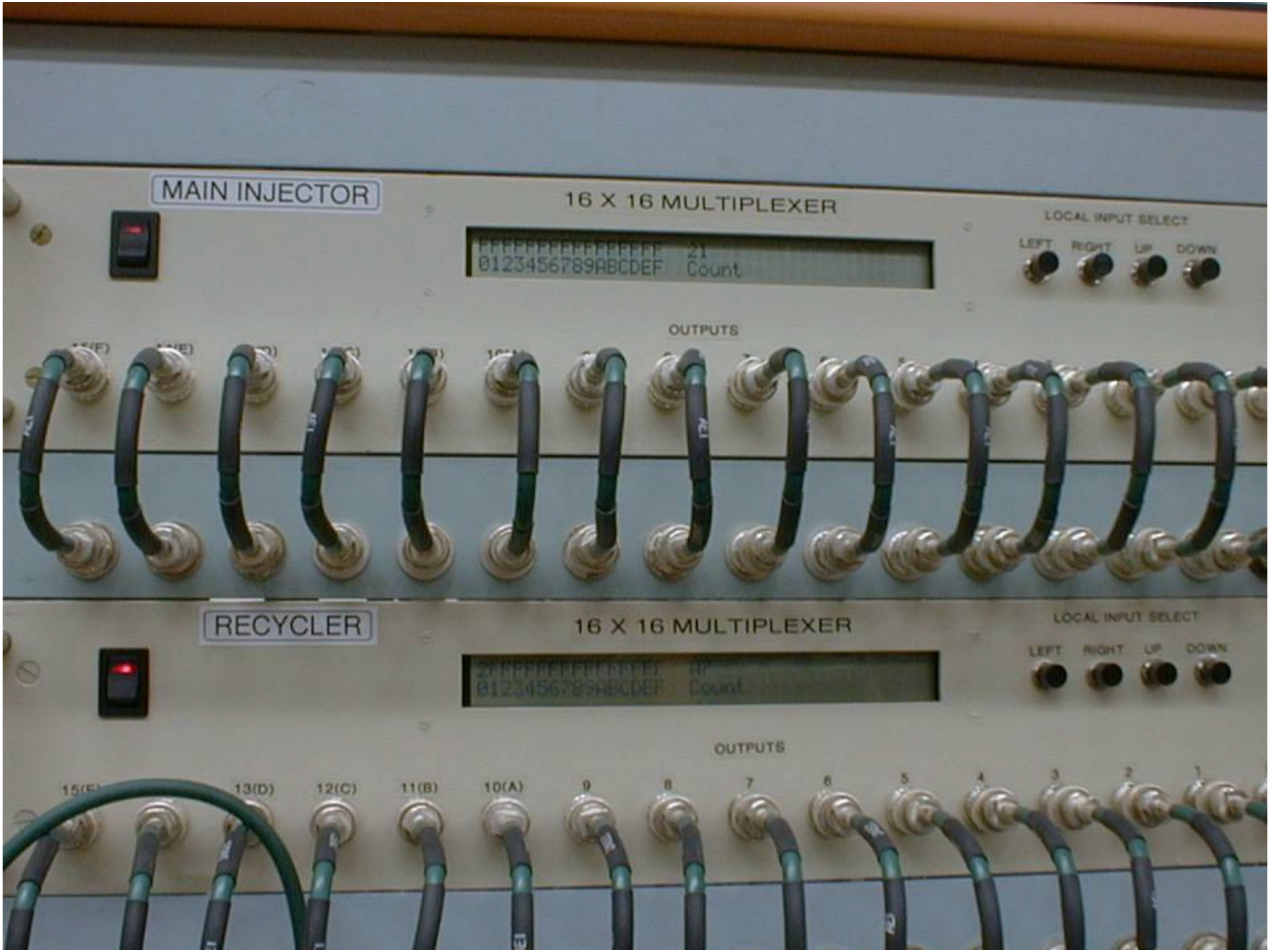
-< 8>+ One+ AUTO F= 600 F= 475.19 , 473.93 , 303.23 , 303.5
fbi.... sbd.... 8gev... ibeam's tune... ipm.... toroid DAMPERS
-I:DDCMSS Damper MI State Selec 0 0
! BEAM PINGER TIMER REGISTERS
! PINGER ACTIVE SIGNAL
I:DDXPAC X Dampr Pinger Active 0
I:DDYPAC Y Dampr Pinger Active 0
I:DDZPAC Z Dampr Pinger Active 0
! PINGER 1ST TURN TO ACTIATE
-I:DDXP1T X Dampr Pinger 1st Tu 0 0
-I:DDYP1T Y Dampr Pinger 1st Tu 0 0
-I:DDZP1T Z Dampr Pinger 1st Tu 0 0
! PINGER LENGTH IN TURNS TO STAY ACTIVE
-I:DDXPLT X Dampr Pinger Len.Tu 0 0
-I:DDYPLT Y Dampr Pinger Len.Tu 0 0
-I:DDZPLT Z Dampr Pinger Len.Tu 0 0
!PINGER 1ST BUCKET TO HIT
-I:DDXP1B X Dampr Pinger 1st Bk 0 0
-I:DDYP1B Y Dampr Pinger 1st Bk 0 0
-I:DDZP1B Z Dampr Pinger 1st Bk 0 0
! PINGER LENGTH IN BUCKETS TO HIT
-I:DDXPLB X Dampr Pinger Leng. 0 0
-I:DDYPLB Y Dampr Pinger Leng. 0 0
-I:DDZPLB Z Dampr Pinger Leng. 0 0
! PINGER ACTIVE TURNCOUNTER
I:DDXPAT X Dampr Pinger Turnco 0
I:DDYPAT Y Dampr Pinger Turnco 0
I:DDZPAT Z Dampr Pinger Turnco 0
Java Applet Window

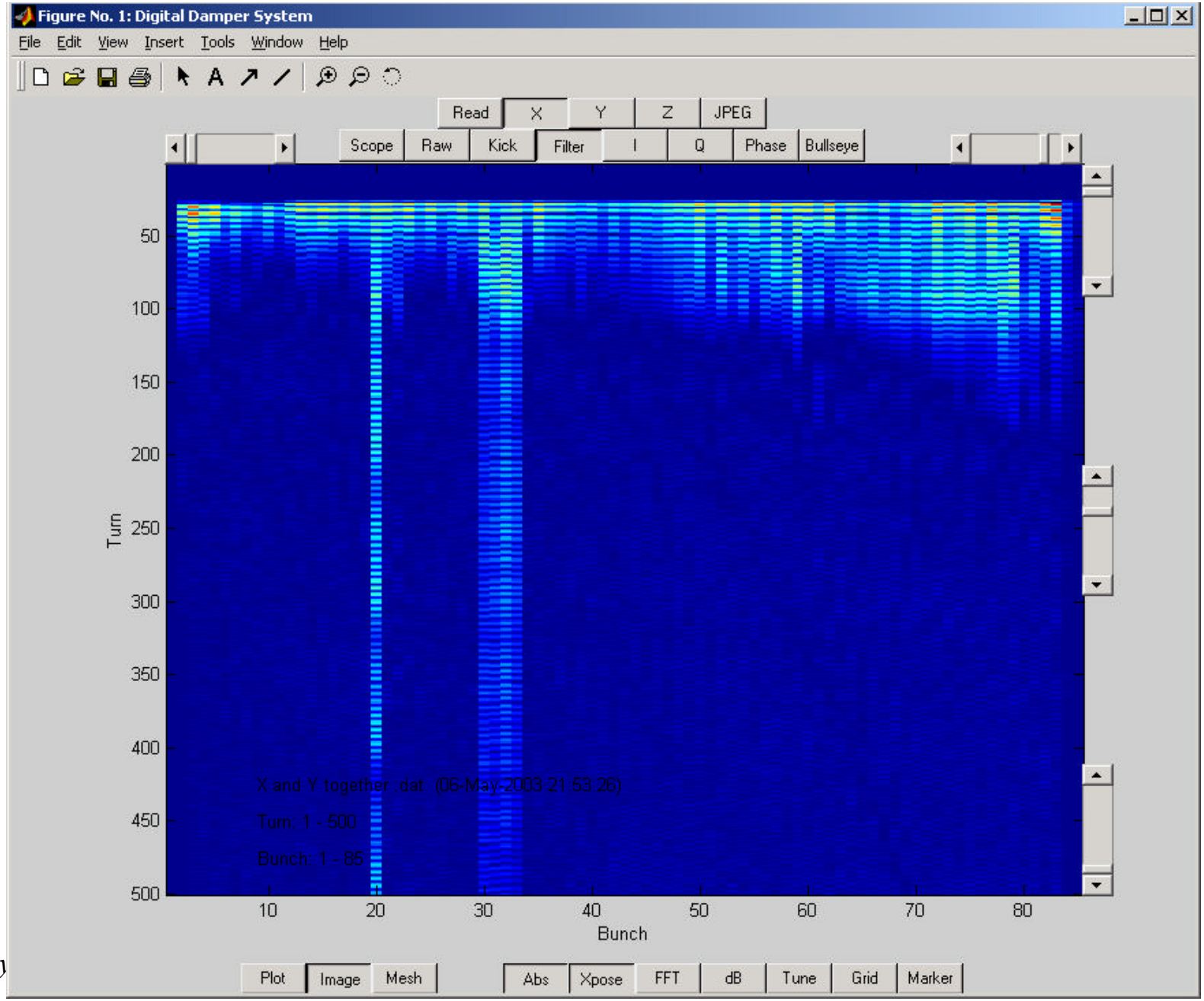

PA:I34 INT MON PARAM<NoSets>
I34 MI60 2.5MHZ BPMS SET D/A A/D Com-U *COPIES*
-<FTP>+ *SA* X-A/D X=TIME Y=E:DYR01G,E:DYR02G,E:DTS01G,E:DTS02G
COMMAND ---- Volts I= 0 I= 475.16 , 473.9 , 303.2 , 303.47
-<10>+ One+ AUTO F= 600 F= 475.19 , 473.93 , 303.23 , 303.5
fbi.... sbd.... 8gev... ibeam's tune... ipm.... toroid DAMPERS
-I:DDCMSS Damper MI State Selec 0 0
! FIFO DAQ CONTROL REGISTERS
! ----------
! DAQ REQUEST REGISTER [0:30] 1-BIT
-I:DDXQRQ X Dampr DAQ Request B 0 0
-I:DDYQRQ Y Dampr DAQ Request B 0 0
-I:DDZQRQ Z Dampr DAQ Request B 0 0
! DAQ REQUEST STATUS REG: 0=IDLE,1=PENDING,2=ACTIV
I:DDXQRS X Dampr DAQ Req. Stat 0
I:DDYQRS Y Dampr DAQ Req. Stat 0
I:DDZQRS Z Dampr DAQ Req. Stat 0
! DAQ FIFO#0: NOT A GOOD IDEA TO PUT THESE ON PAGE
!I:DDXQF0 X Dampr DAQ FIFO 0 -1 -1
!I:DDYQF0 Y Dampr DAQ FIFO 0 -1 -1
!I:DDZQF0 Z Dampr DAQ FIFO 0 -1 -1
! FIFO #1
!I:DDXQF1 X Dampr DAQ FIFO 1 -1 -1
!I:DDYQF1 Y Dampr DAQ FIFO 1 -1 -1
!I:DDZQF1 Z Dampr DAQ FIFO 1 -1 -1
! DAQ MUX CONTROL REGISTER [0:30]
-I:DDXQM1 X Dampr DAQ Mux 0 0
-I:DDYQM1 Y Dampr DAQ Mux 0 0
-I:DDZQM1 Z Dampr DAQ Mux 0 0
Java Applet Window

25-page User's Manual

- …and counting.
- We are in the market for guinea pigs to test the documentation on.
- Plan is to have comprehensive self-test and calibration software.

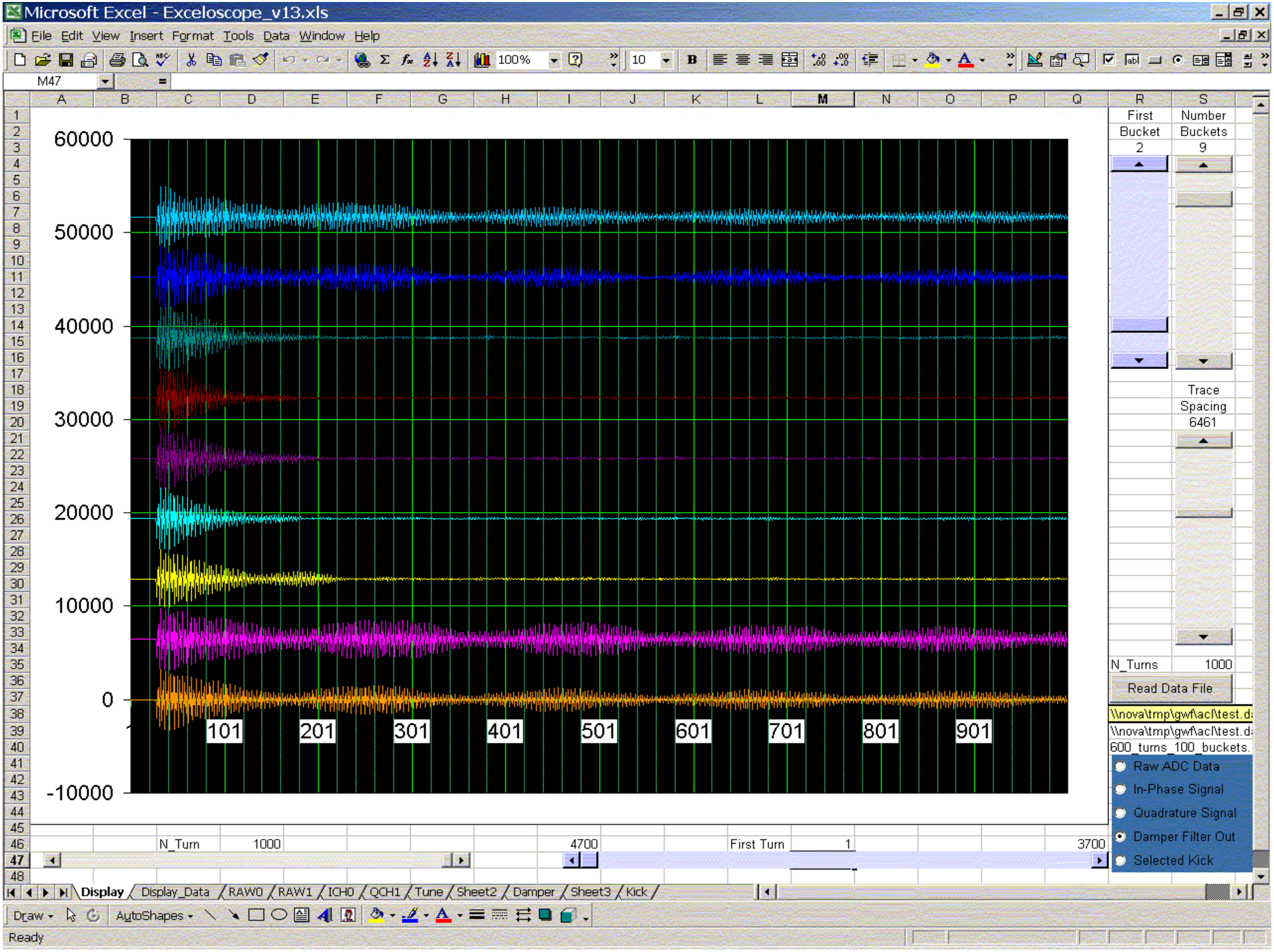

MAIN INJECTOR
16 X 16 MULTIPLEXER
0123456789ABCDEF Count
LOCAL INPUT SELECT
LEFT
RIGHT
UP
DOWN
OUTPUTS
RECYCLER
16 X 16 MULTIPLEXER
0123456789ABCDEF Count
LOCAL INPUT SELECT
LEFT
RIGHT
UP
DOWN
OUTPUTS
13(D)
12(C)
11(B)
10(A)

Damper Display GUI (Matlab) -*W. Schappert*



Other Displays Used:

- D27 (provides real-time scope of RWM)
- Guan Wu's Array Display/File Write
- ACL Script writing text file
  - Help from Brian Hendricks and Dennis Nicklaus
  - ✍ "***Excel***iscope"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M47
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40000
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601
701
801
901
First Bucket
2
Number Buckets
9
Trace Spacing
6461
N_Turns
1000
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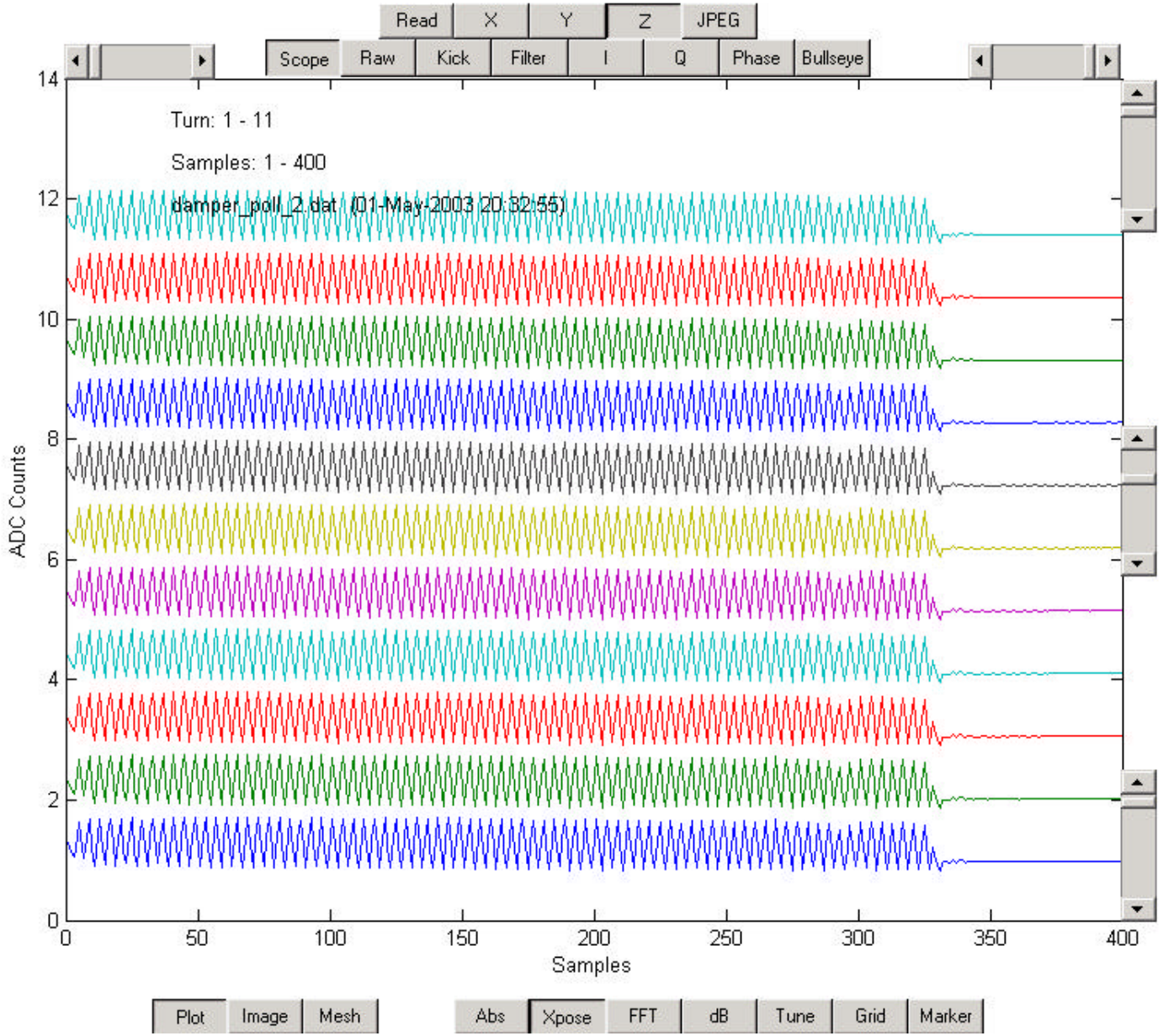
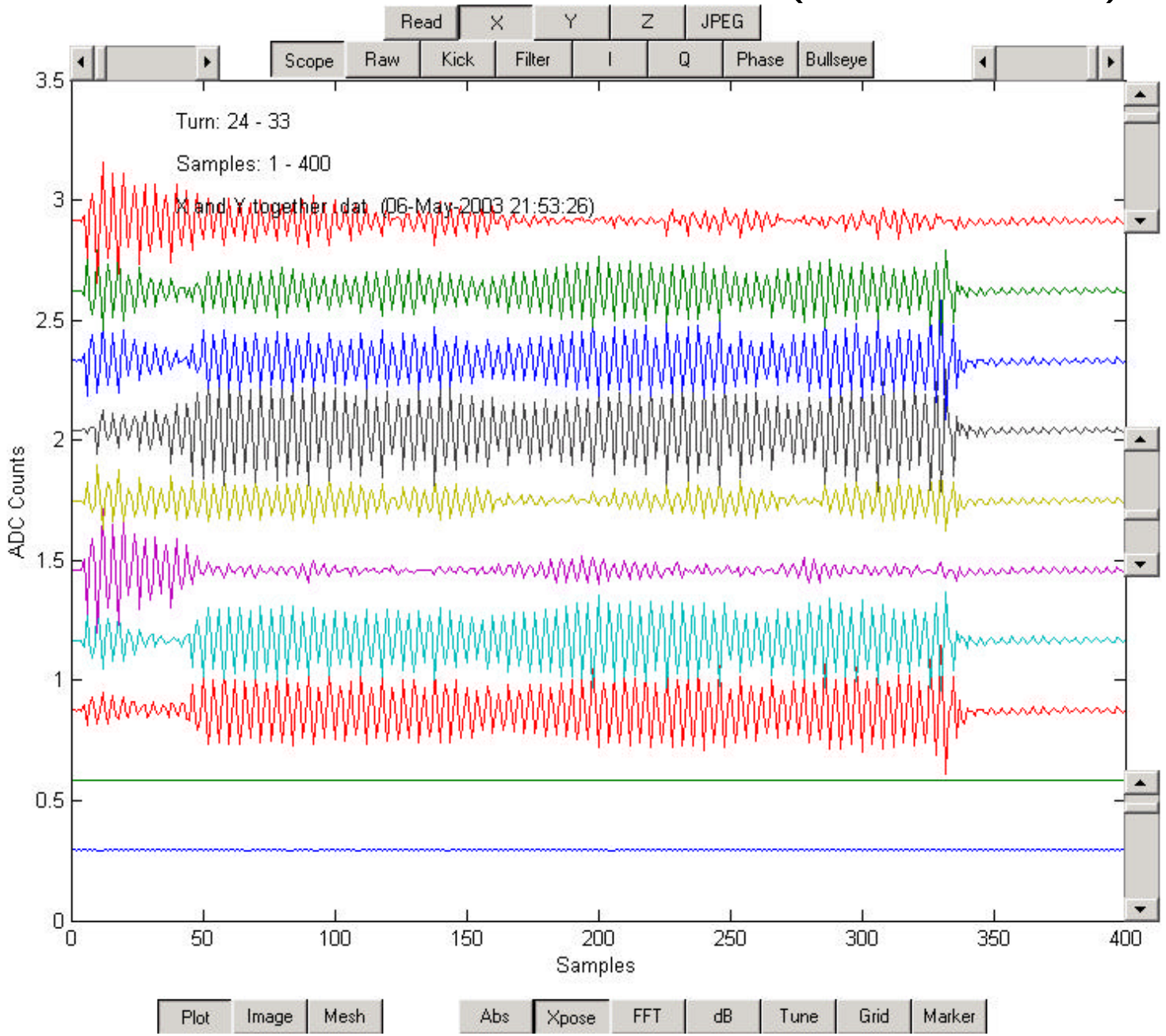
Raw ADC Data
In-Phase Signal
Quadrature Signal
Damper Filter Out
Selected Kick
N_Turn
1000
4700
First Turn
1
3700
Display
Display_Data
RAW0
RAW1
ICH0
QCH1
Tune
Sheet2
Damper
Sheet3
Kick
Draw
AutoShapes
Ready

Longitudinal RAW ADC Waveform

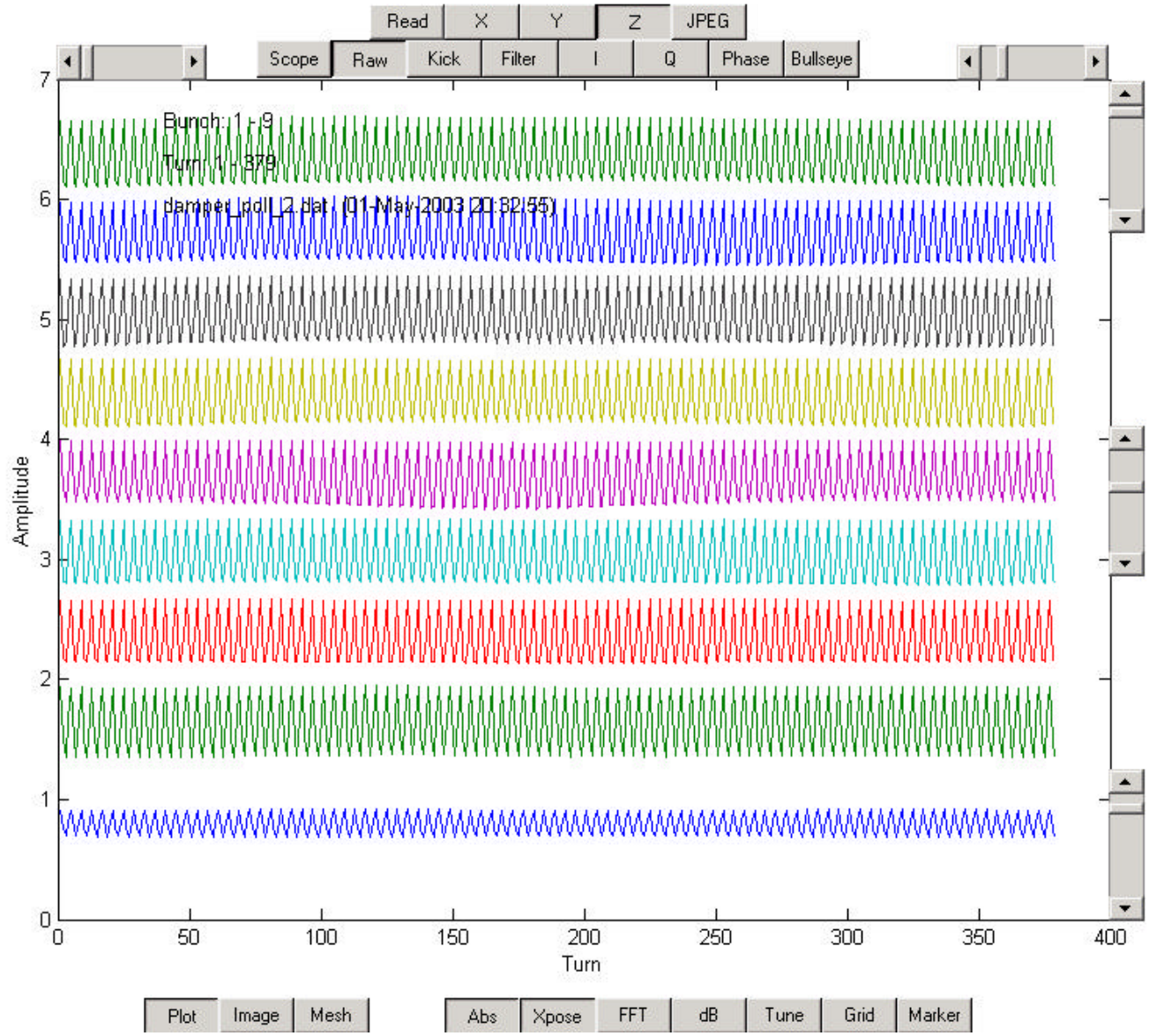
Wall-Current Monitor @212 MHz "Virtual Oscilliscope" in FPGA Firmware



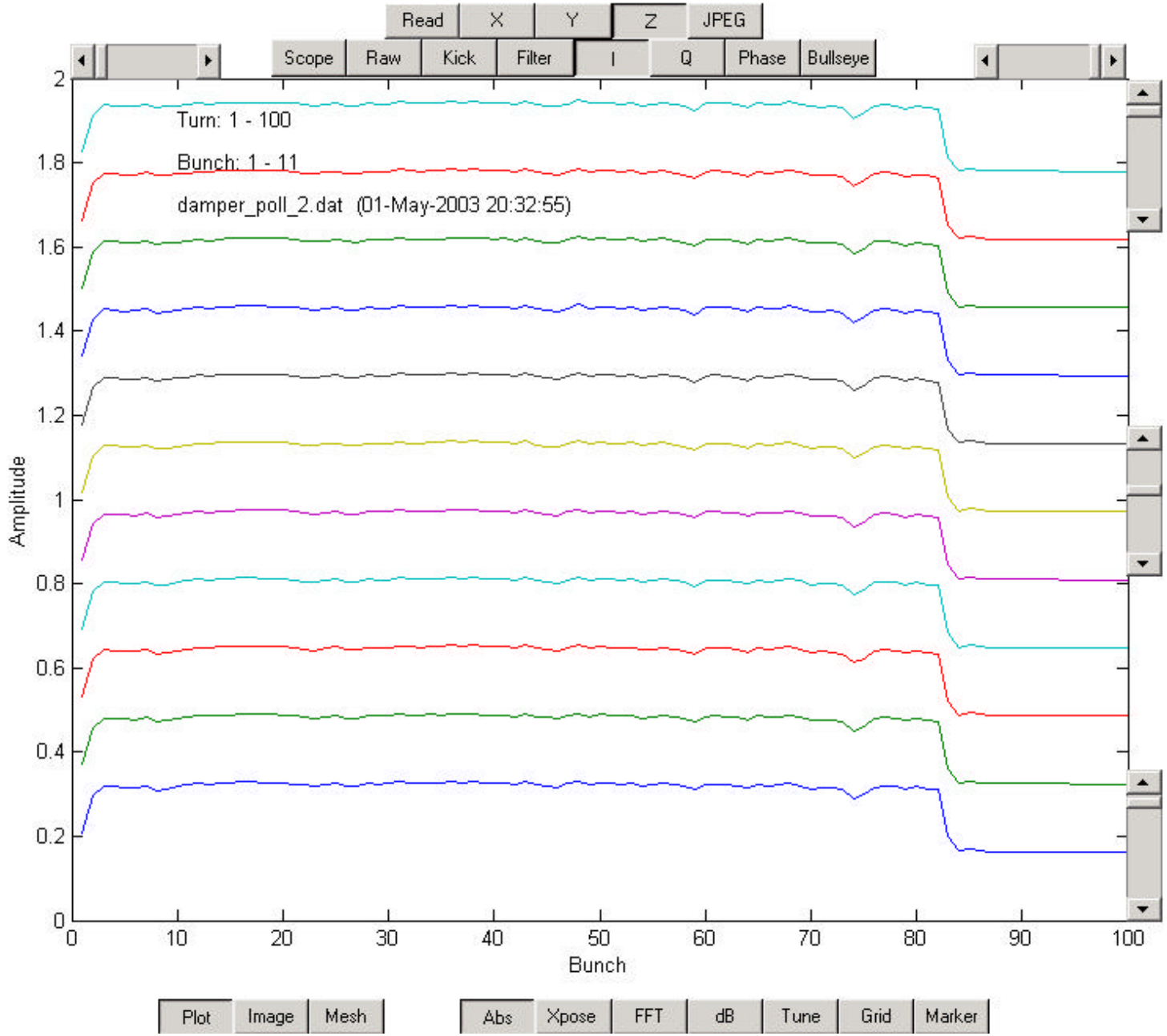
Transverse Waveform (H602 ?)



Bunch by Bunch Time History



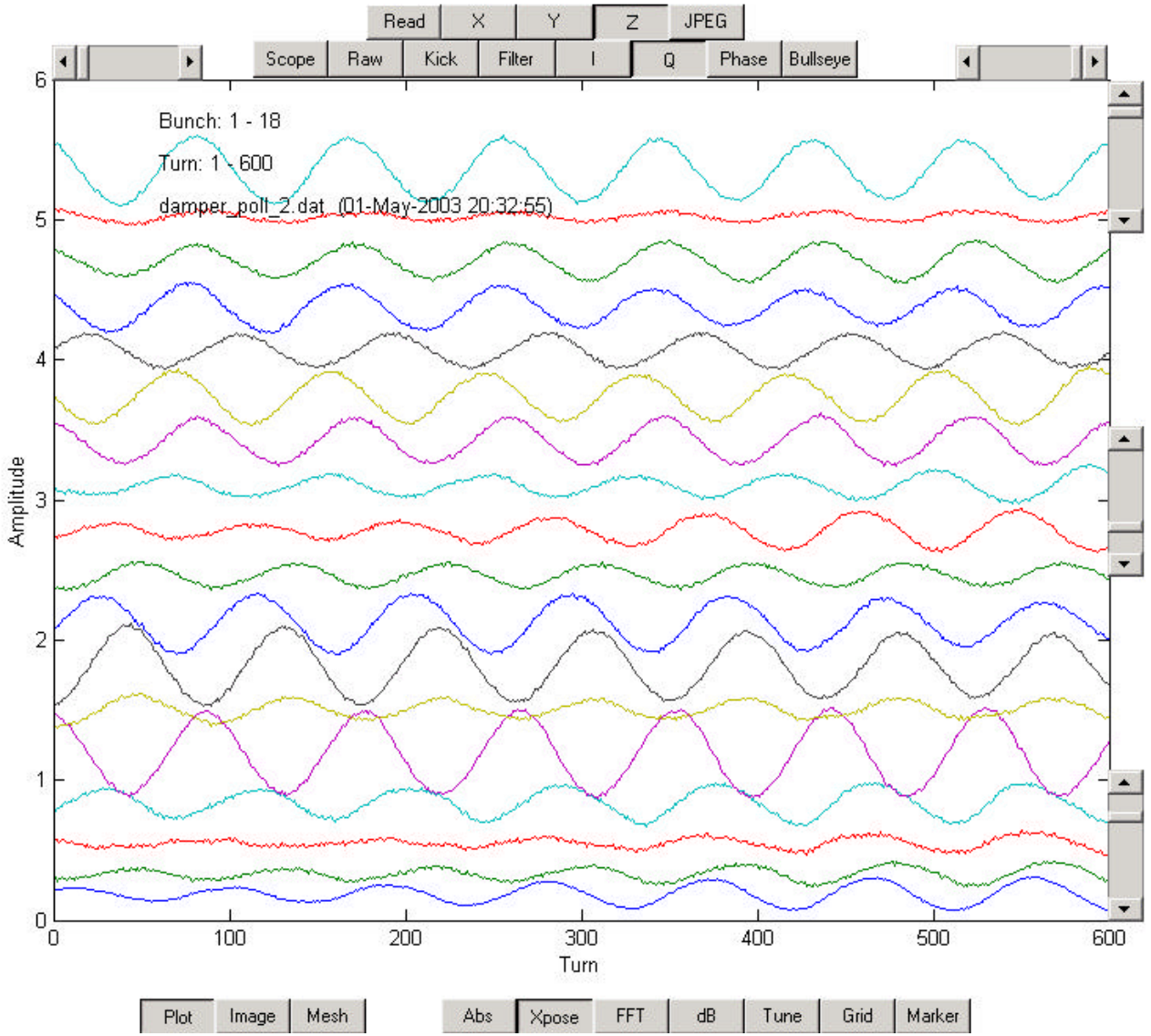
Longitudinal In-Phase vs. Bunch Number



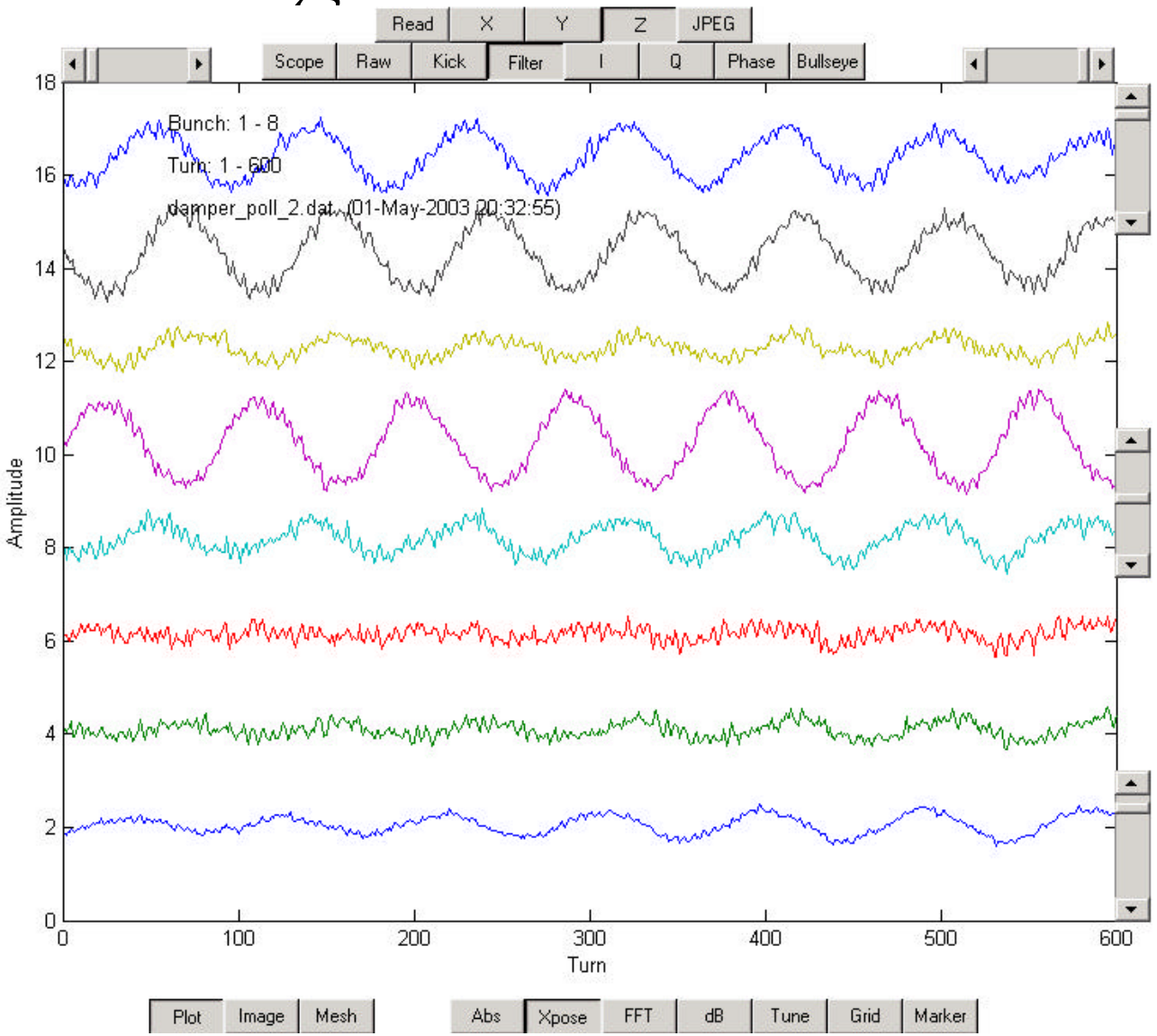
Bunch-By-Bunch Phase

(Longitudinal Quadrature Signal)

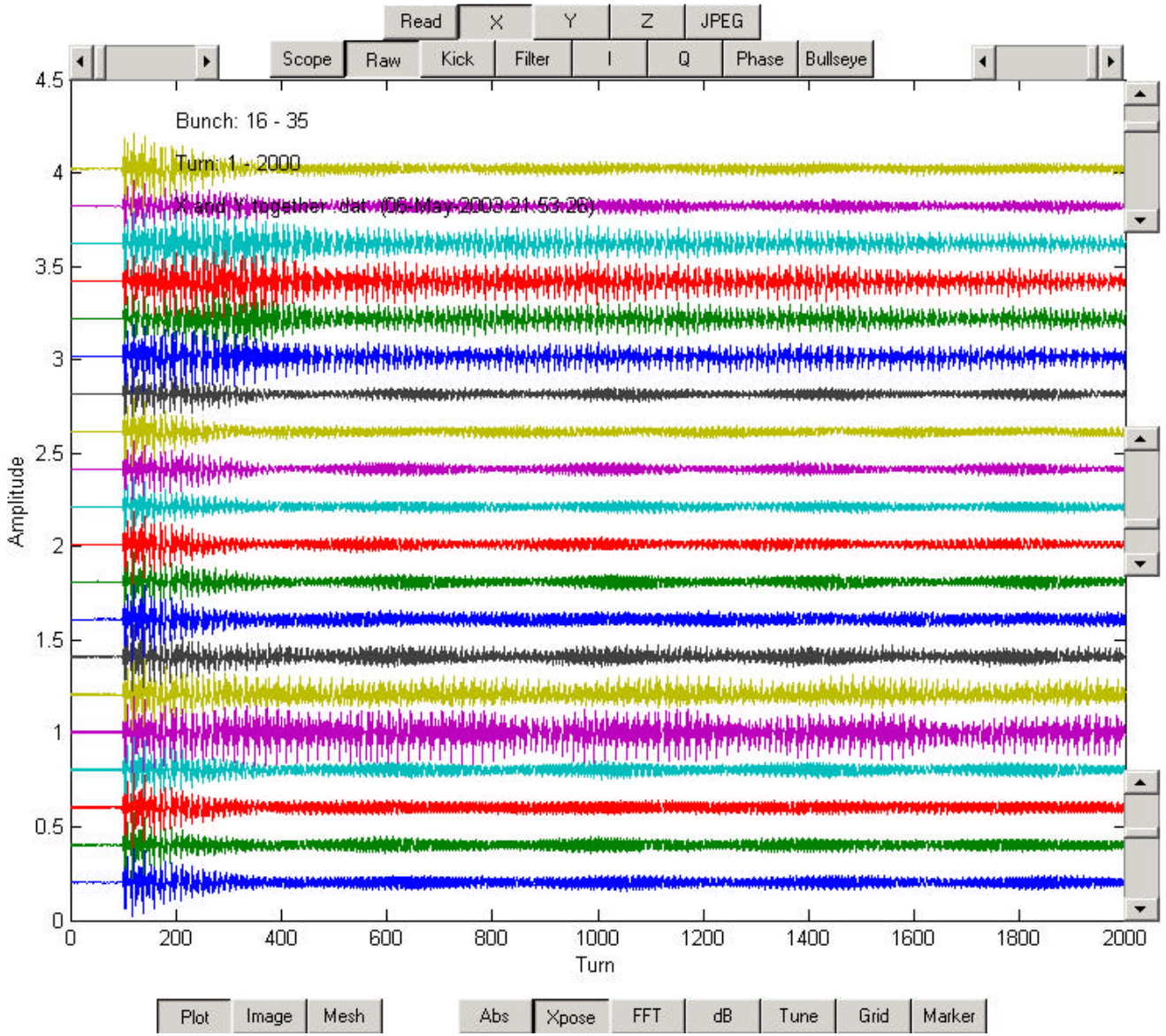
vs. Turn Number



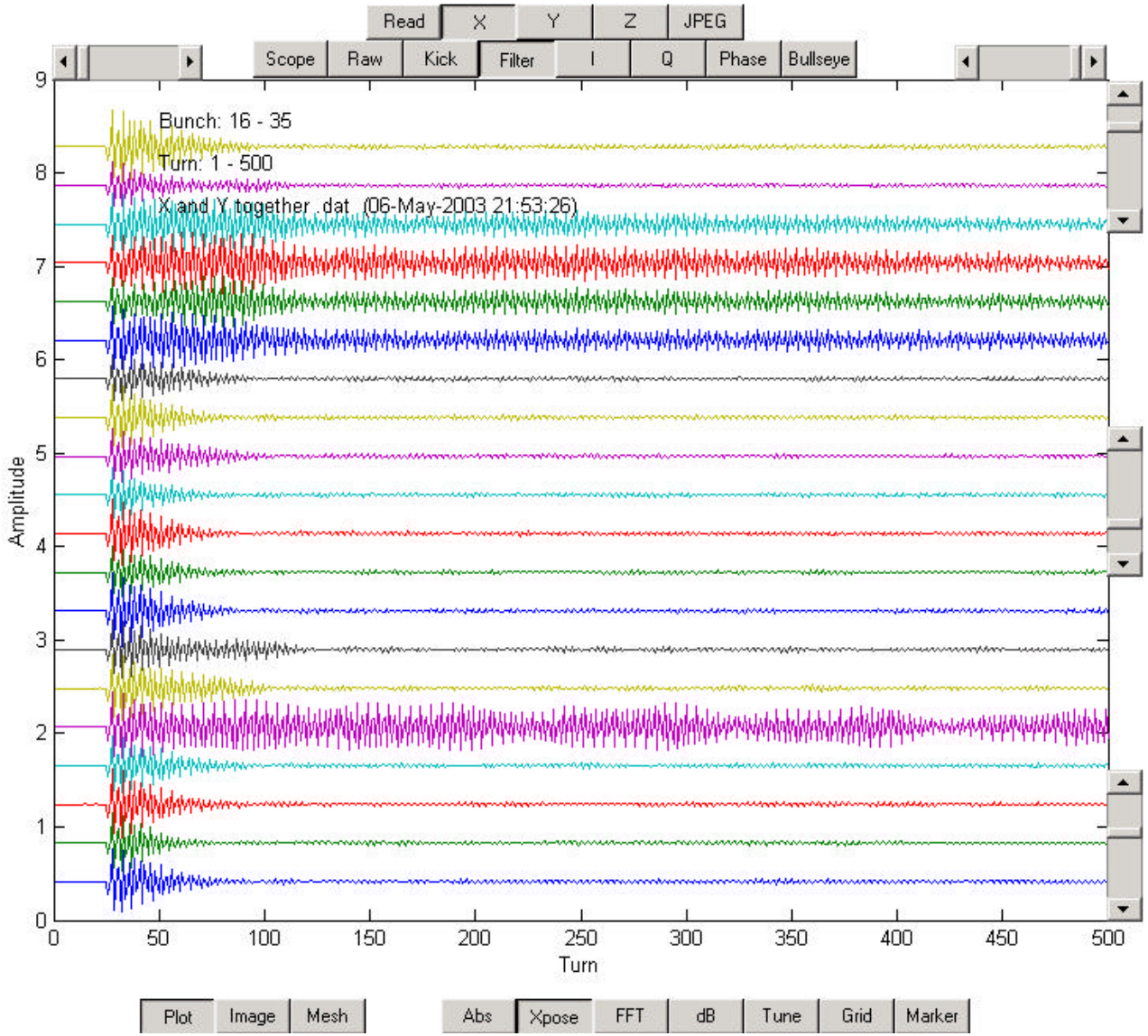
Longitudinal Filter



Raw Waveform for Undamped, Damped and Anti-Damped Bunches (transverse)

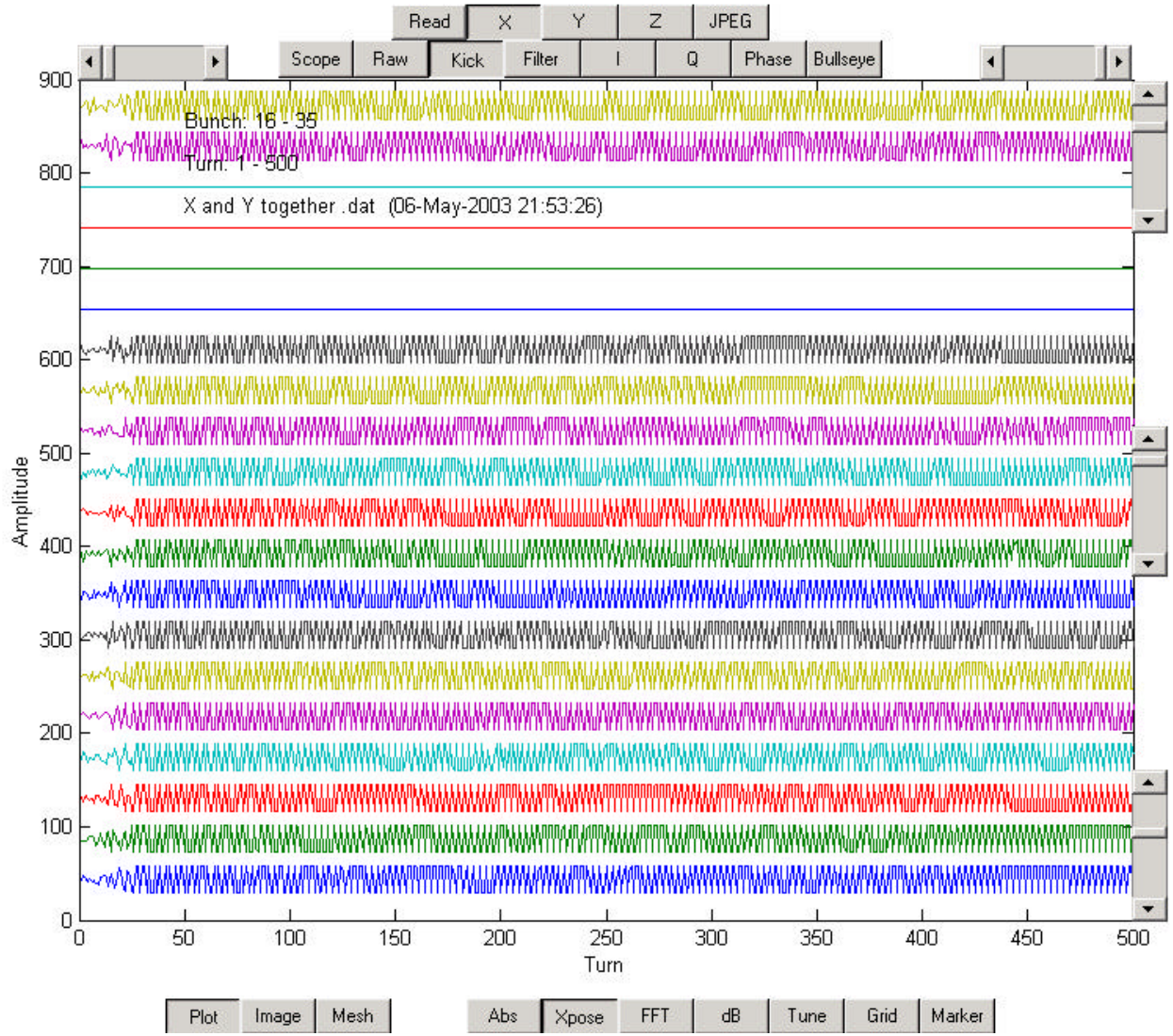


Filter for Undamped, Damped, and Anti-Damped Bunches

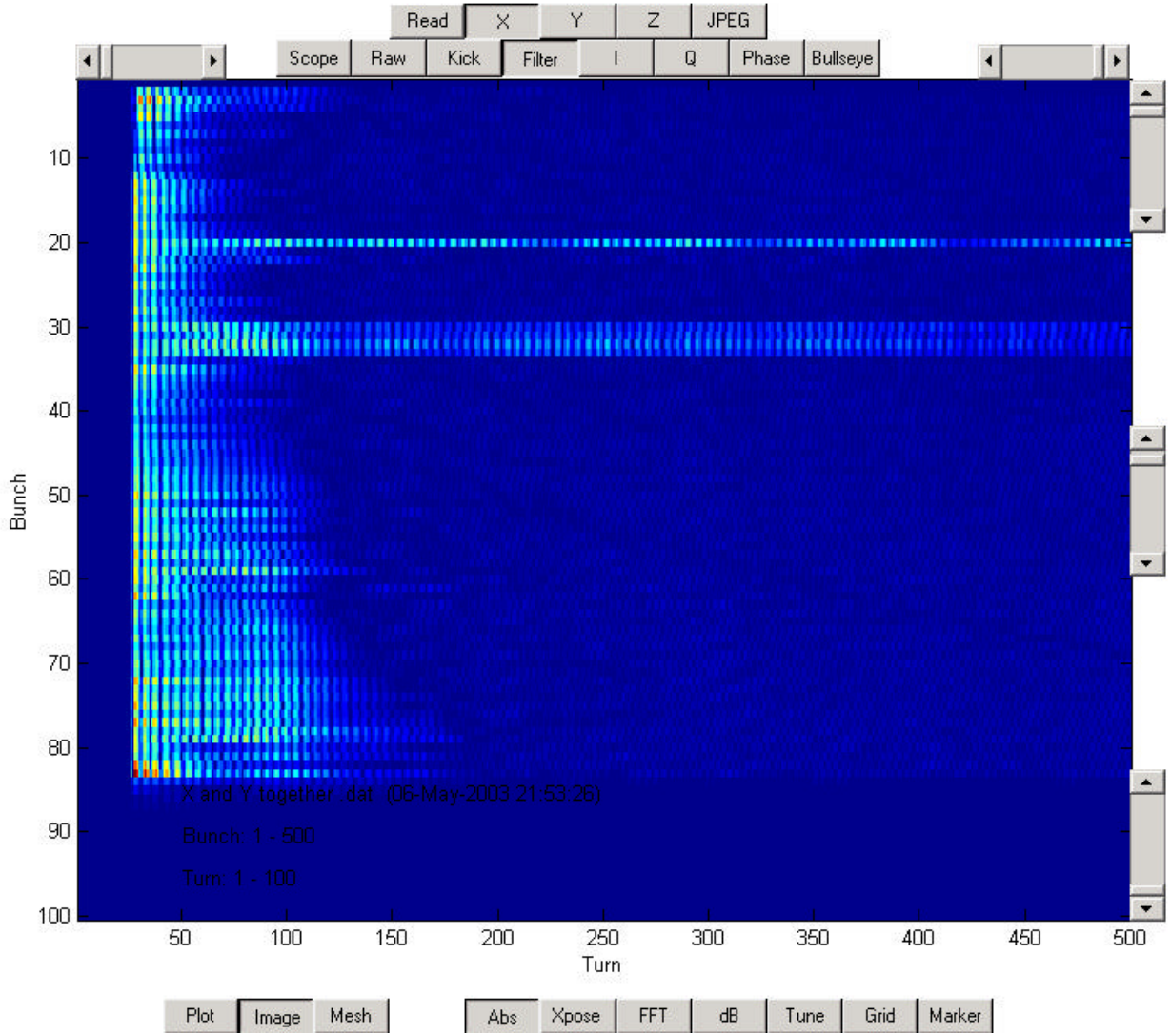


Blowing Selected Bunches out of the Machine (in X,Y, or both)

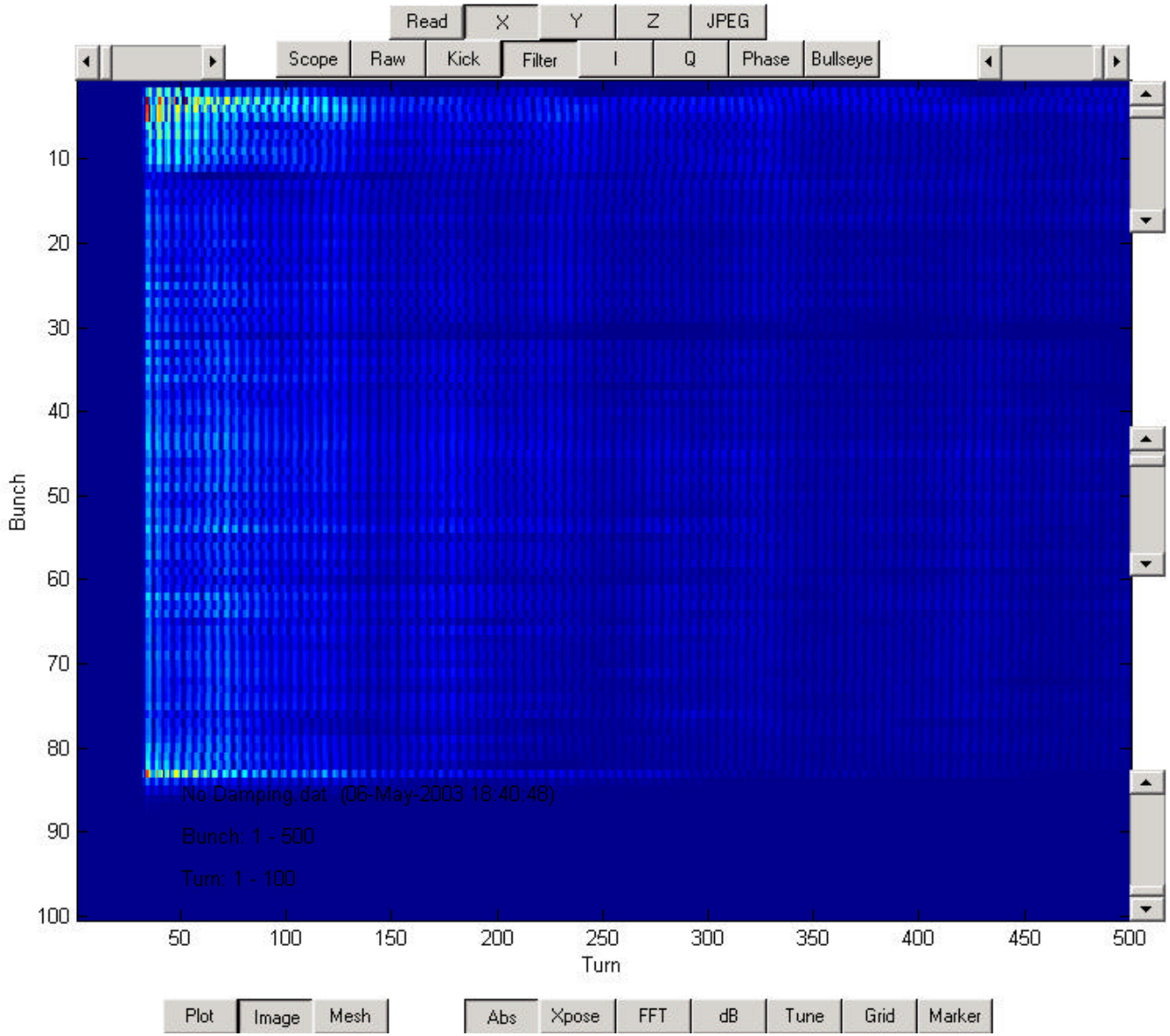
Kick for Undamped, Damped and Anti-Damped Bunches



Undamped, Damped, and Anti-Damped Bunches



No Damping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70
80
90
100
No Damping.dat (06-May-2003 18:40:48)
Bunch: 1 - 500
Turn: 1 - 100
50
100
150
200
250
300
350
400
450
500
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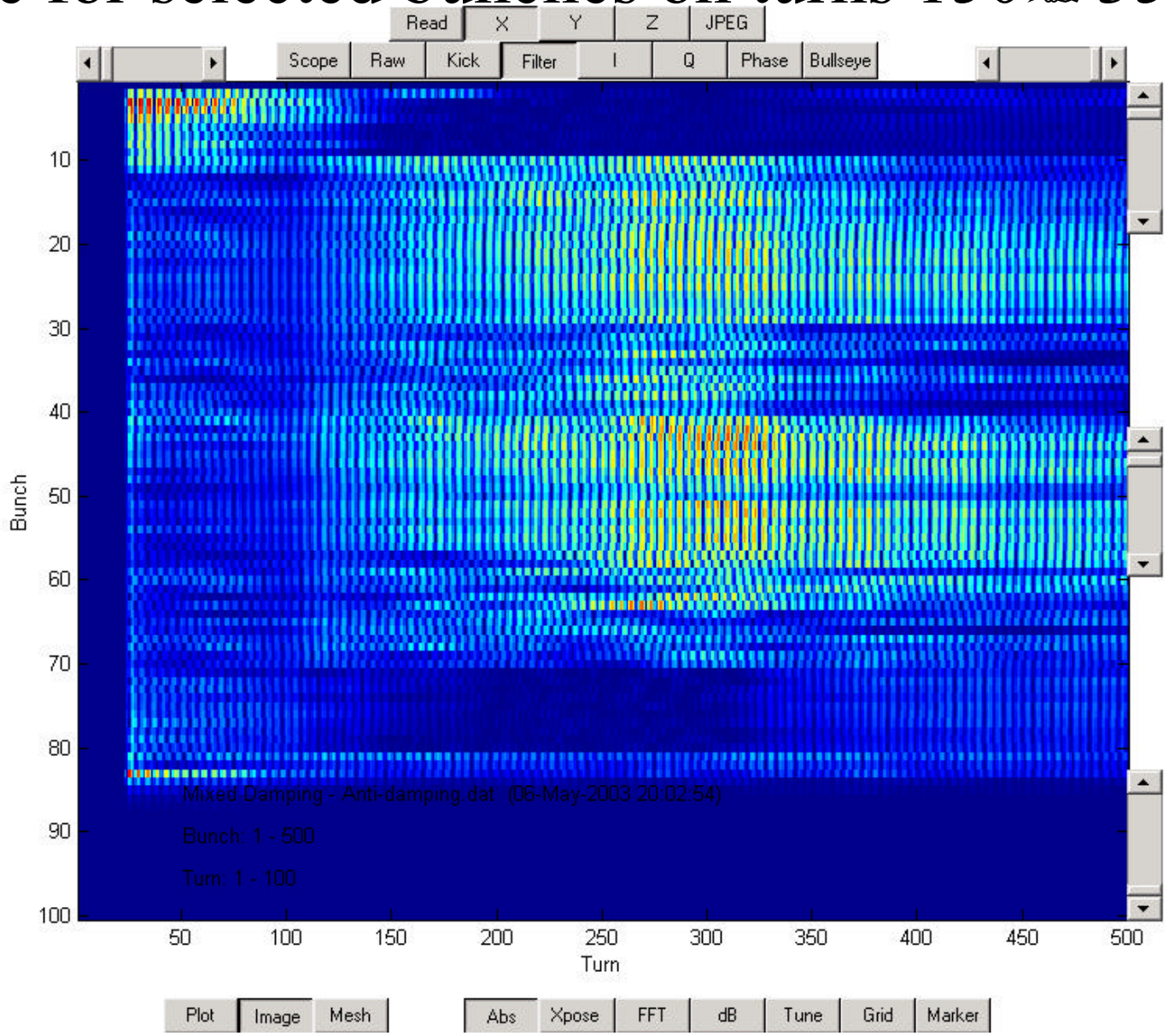
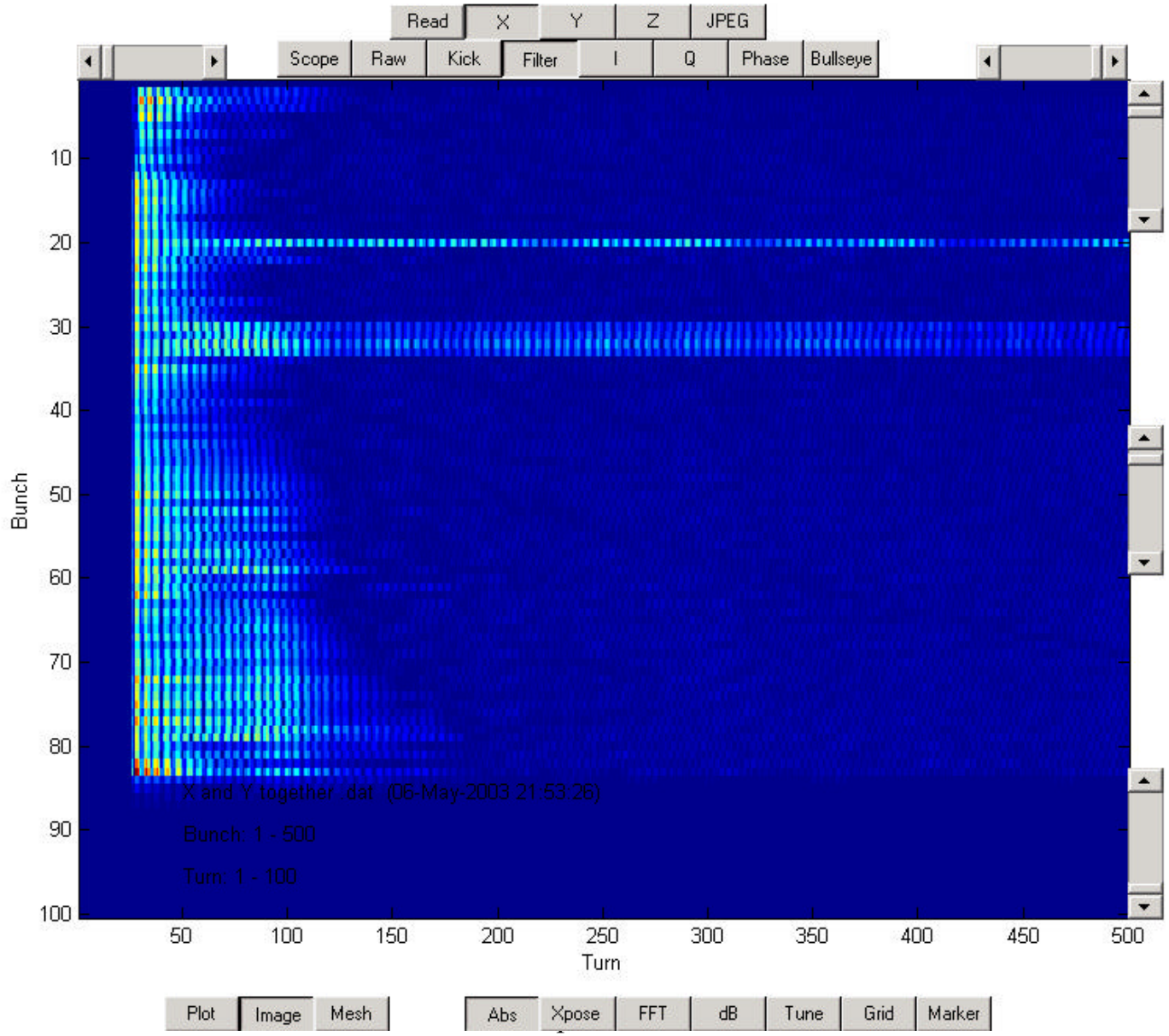
Mesh
Abs
Xpose
FFT
dB
Tune
Grid
Marker

Anti-Damping

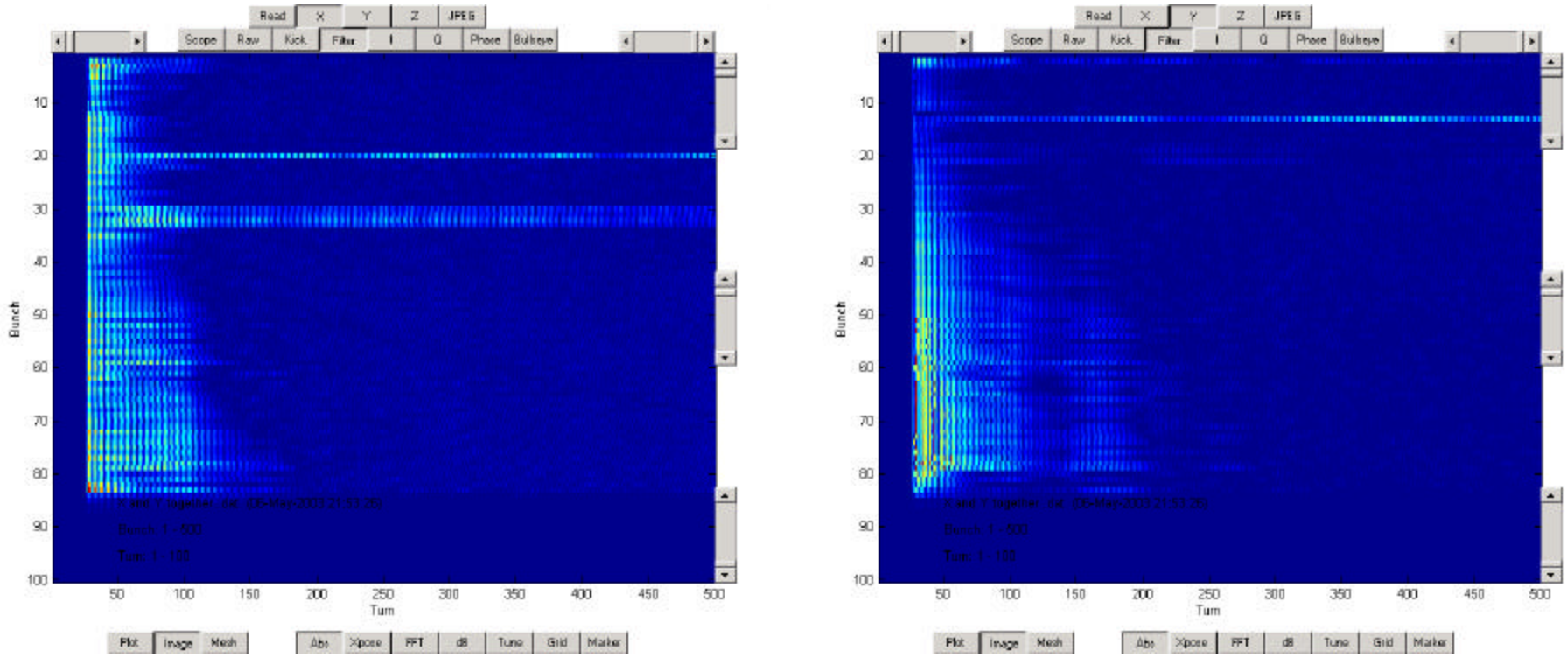
(active for selected bunches on turns 150 ✍ 350)



Bunch-By-Bunch Damping



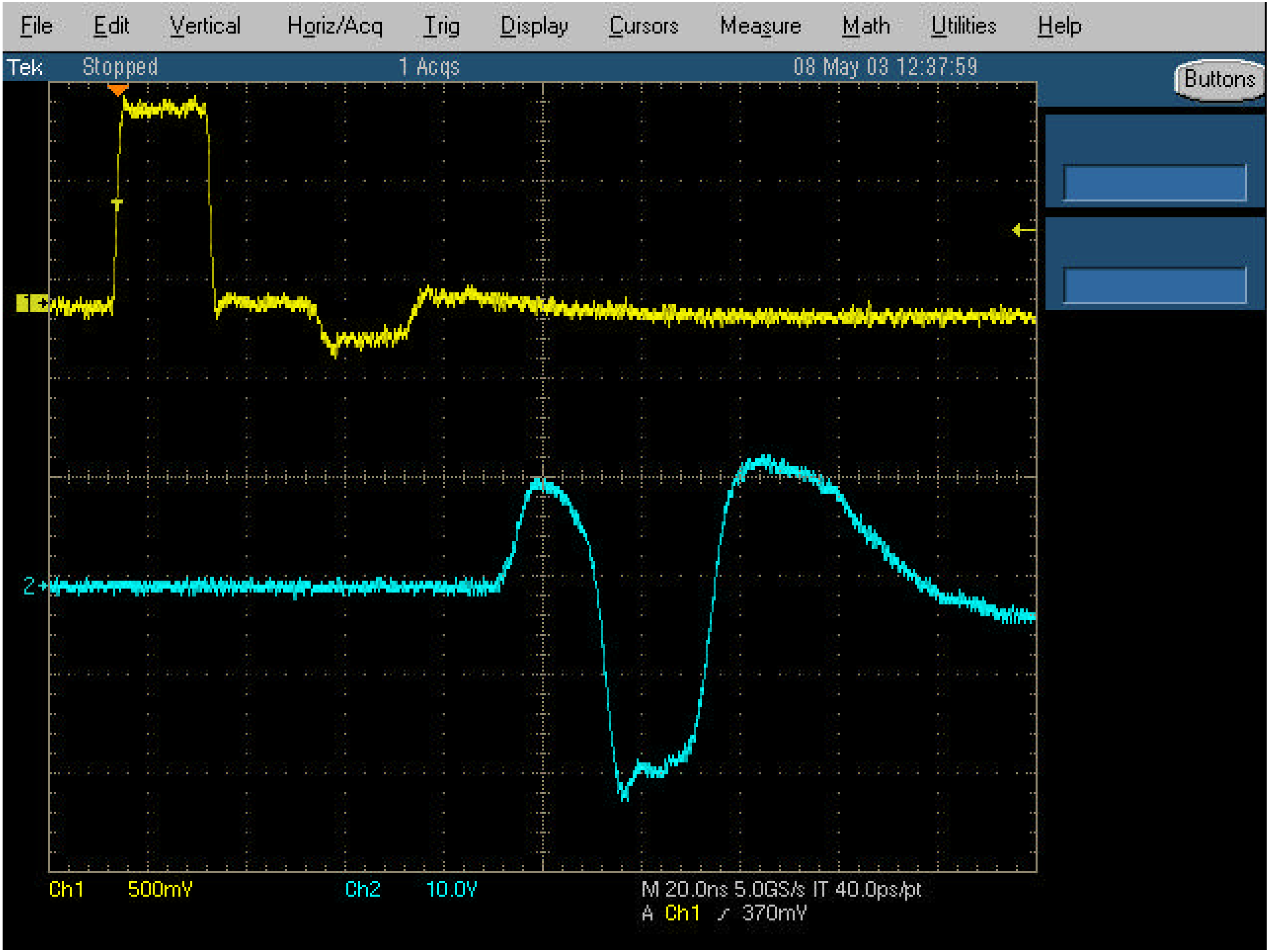
Simultaneous X and Y Damping



Transverse Amplifier Situation

- Existing Transverse Amplifiers cannot provide clean bunch-by-bunch kick
- Alternative ENI Amps have ~2/3 voltage but slew-rate limits
- Overdriving the ENIs (~saturated switches) provided a workable system in short term
- Possibly we want to buy better amps in long term, (or digital switch drivers)

Existing INTECH Amps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Buttons
2+
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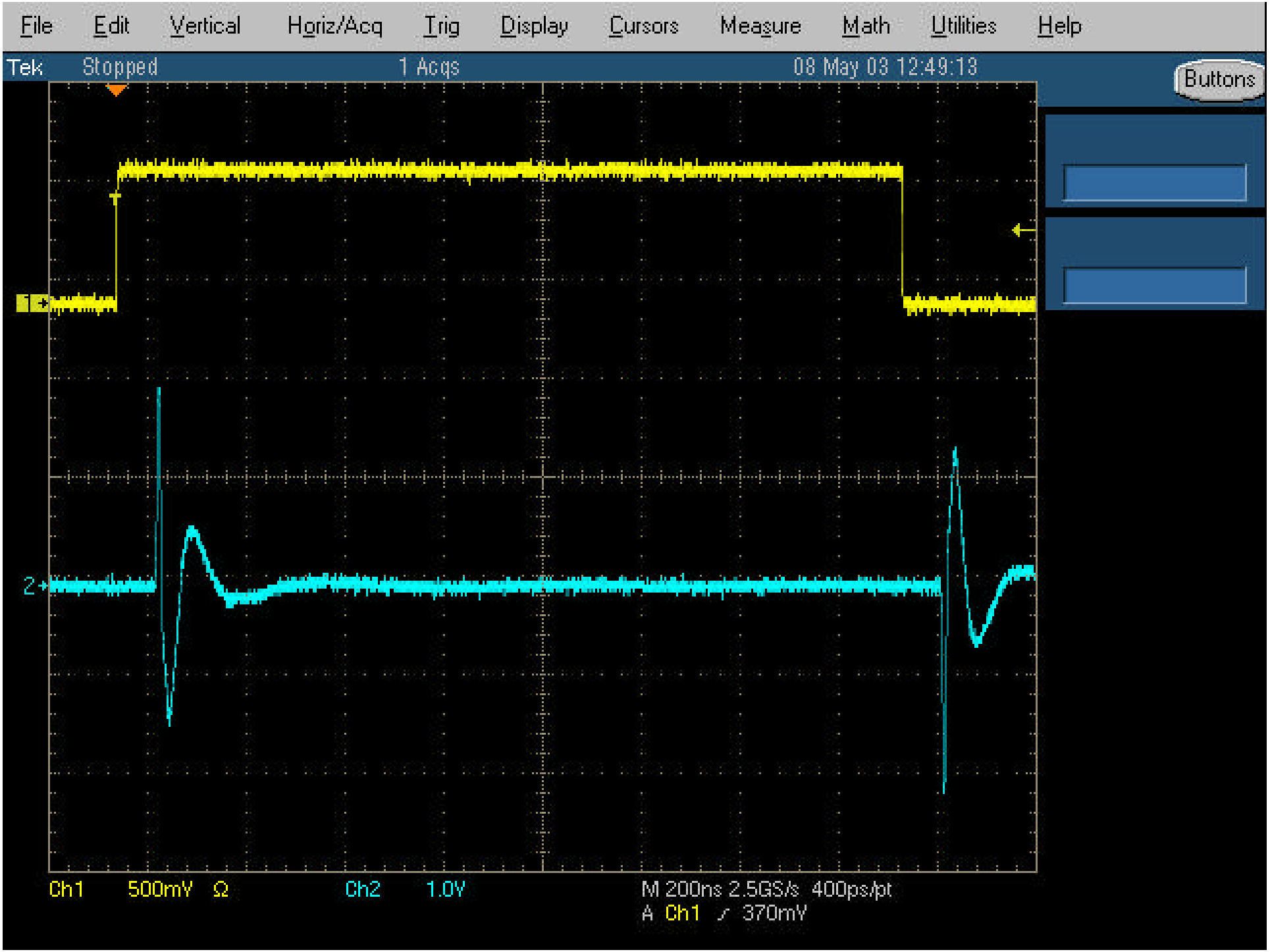
Ch2 10.0V
M 20.0ns 5.0GS/s IT 40.0ps/pt
A Ch1 ⟋ 370mV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2
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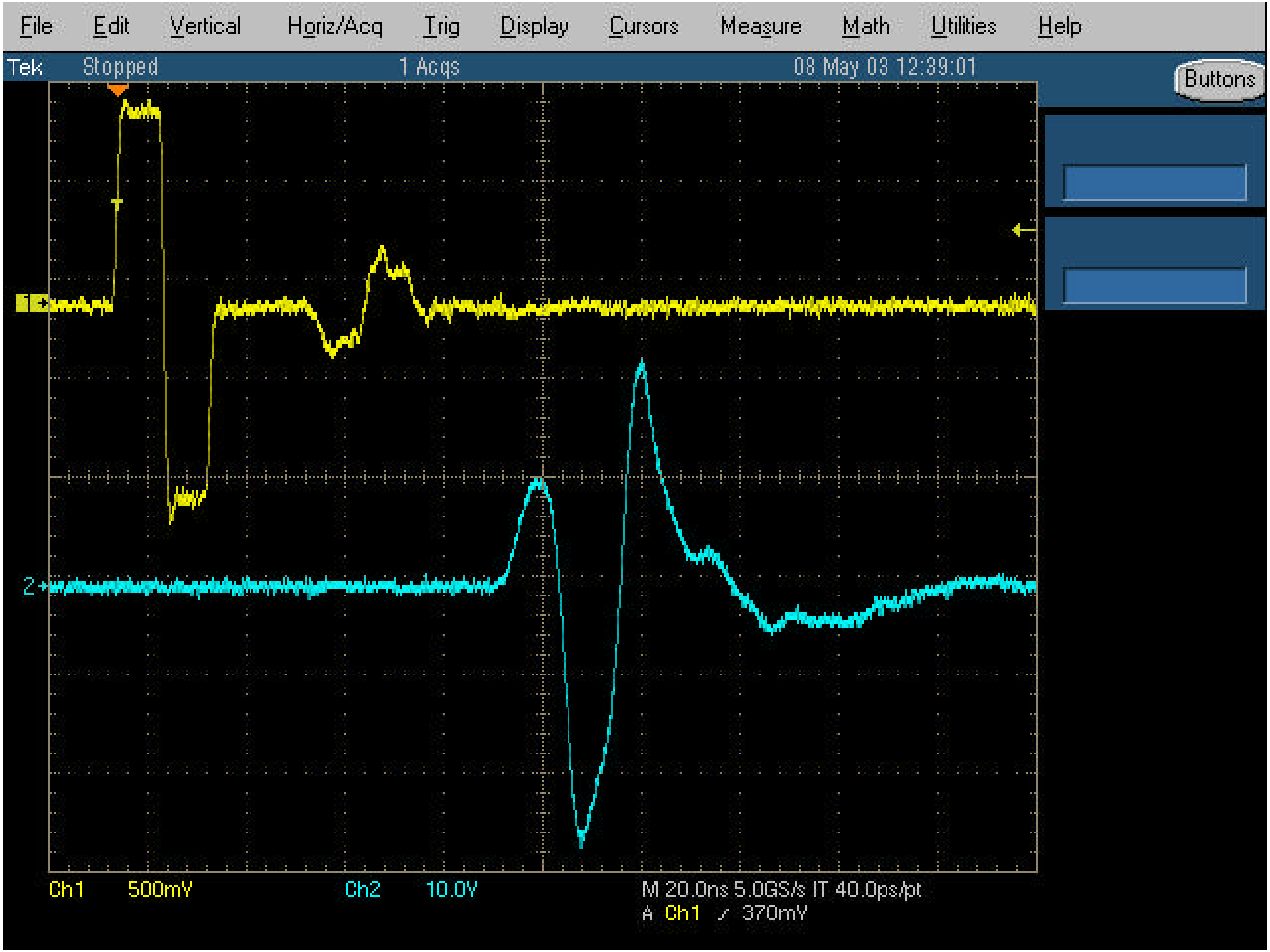
M 200ns 2.5GS/s 400ps/pt
A Ch1 ⟋ 370mV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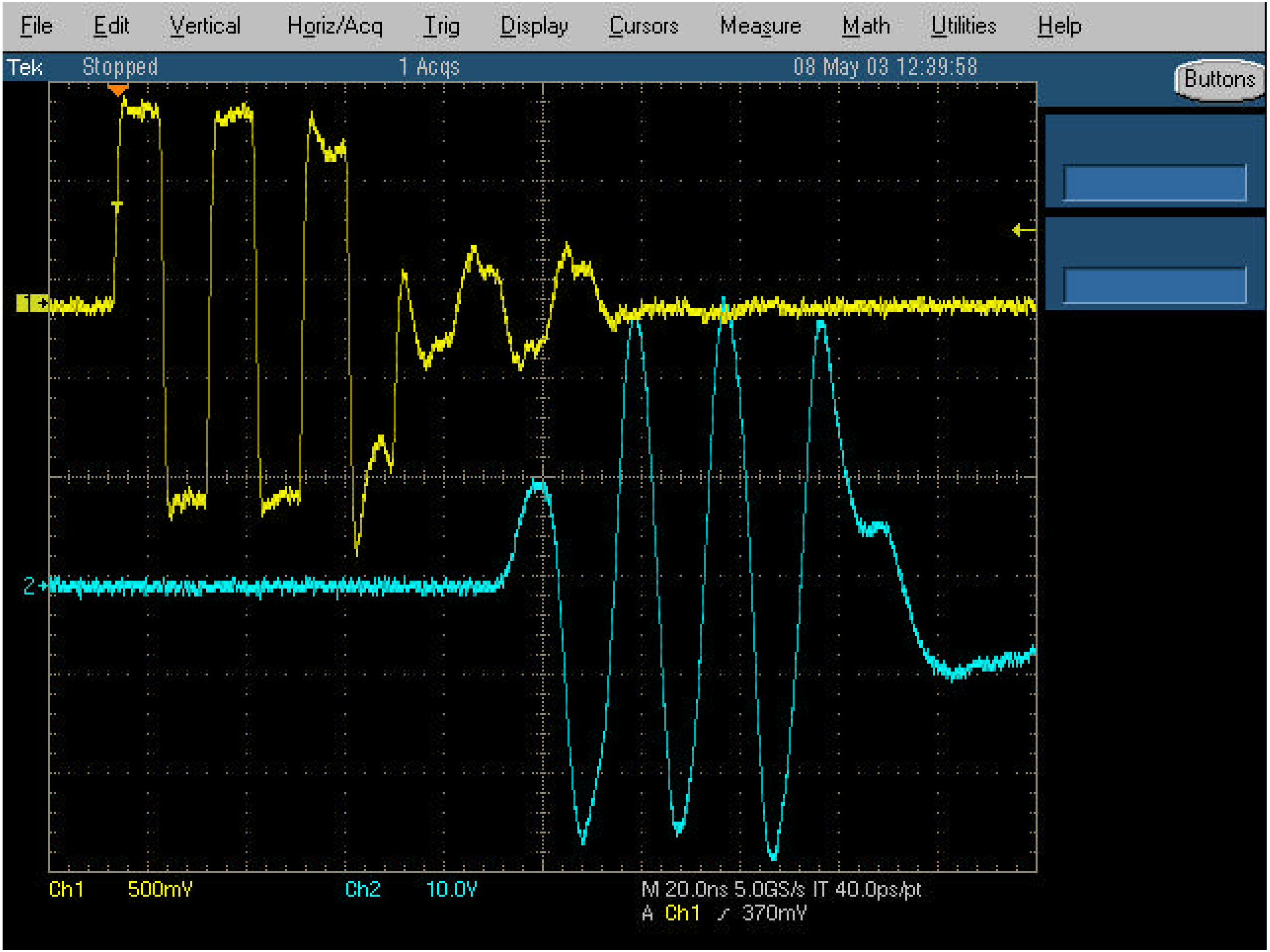
A Ch1 ⟋ 370mV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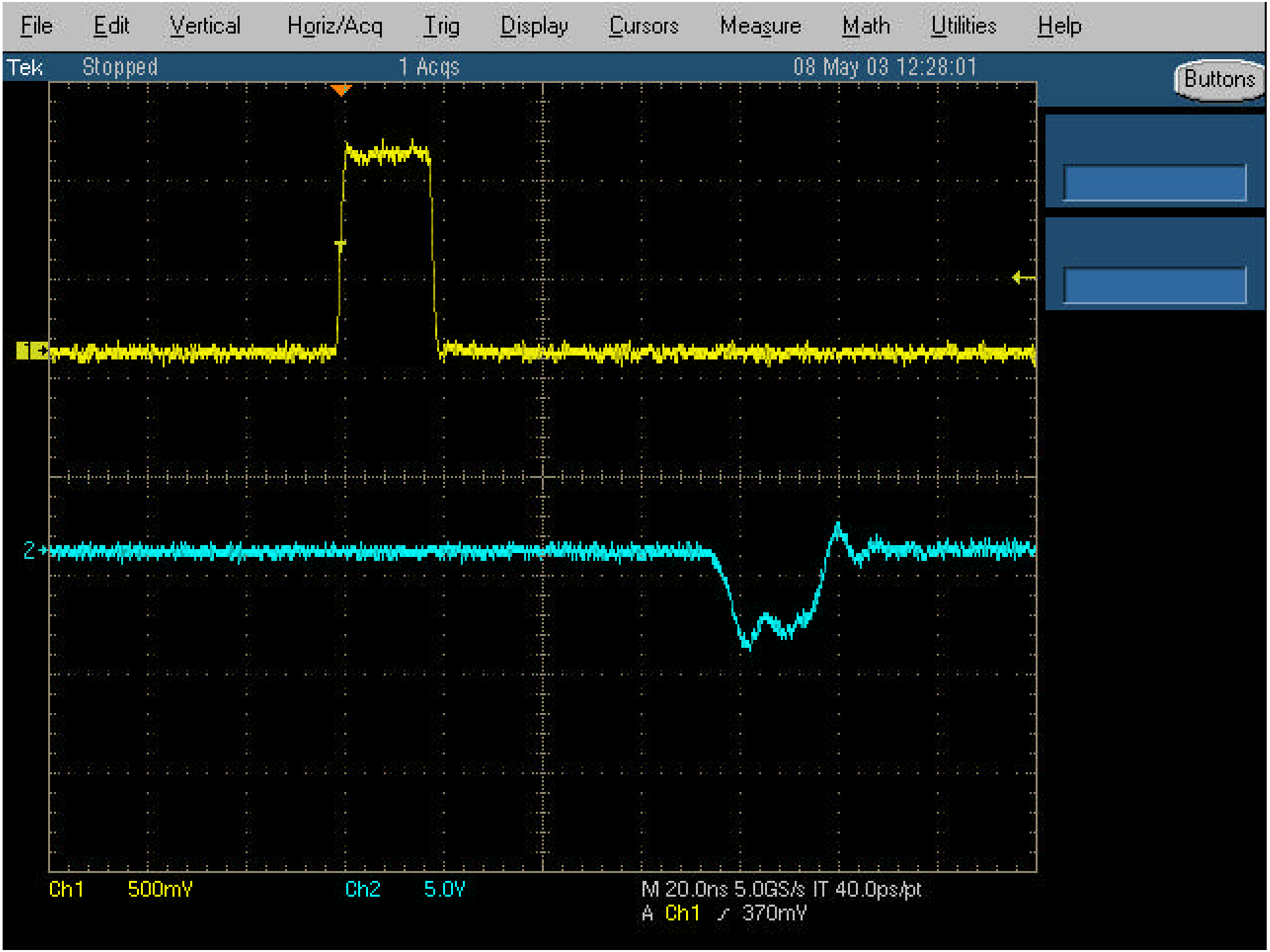
A Ch1 ⟋ 370mV

SWITCHED TO "SPARE" ENI AMPS

Foster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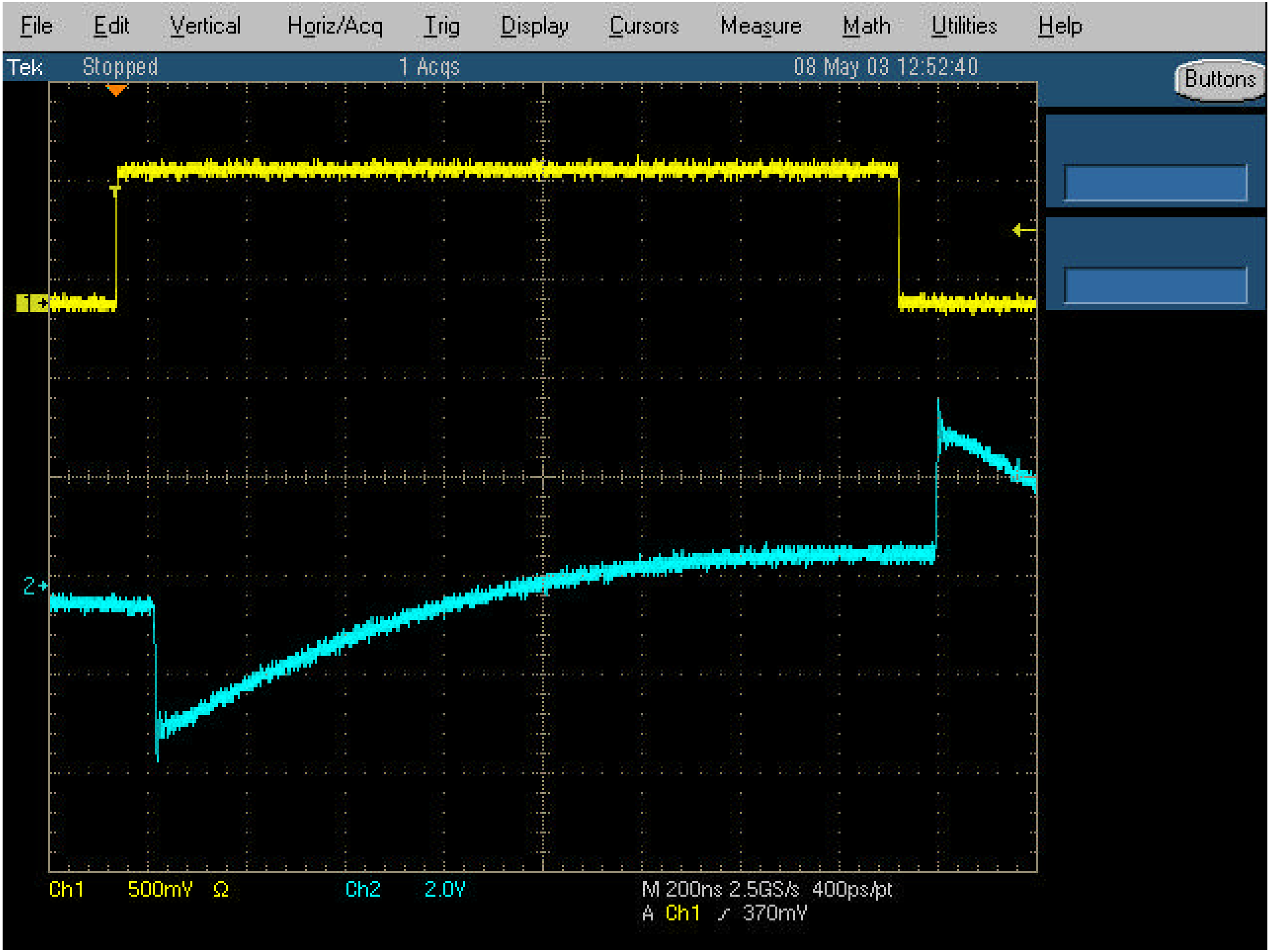
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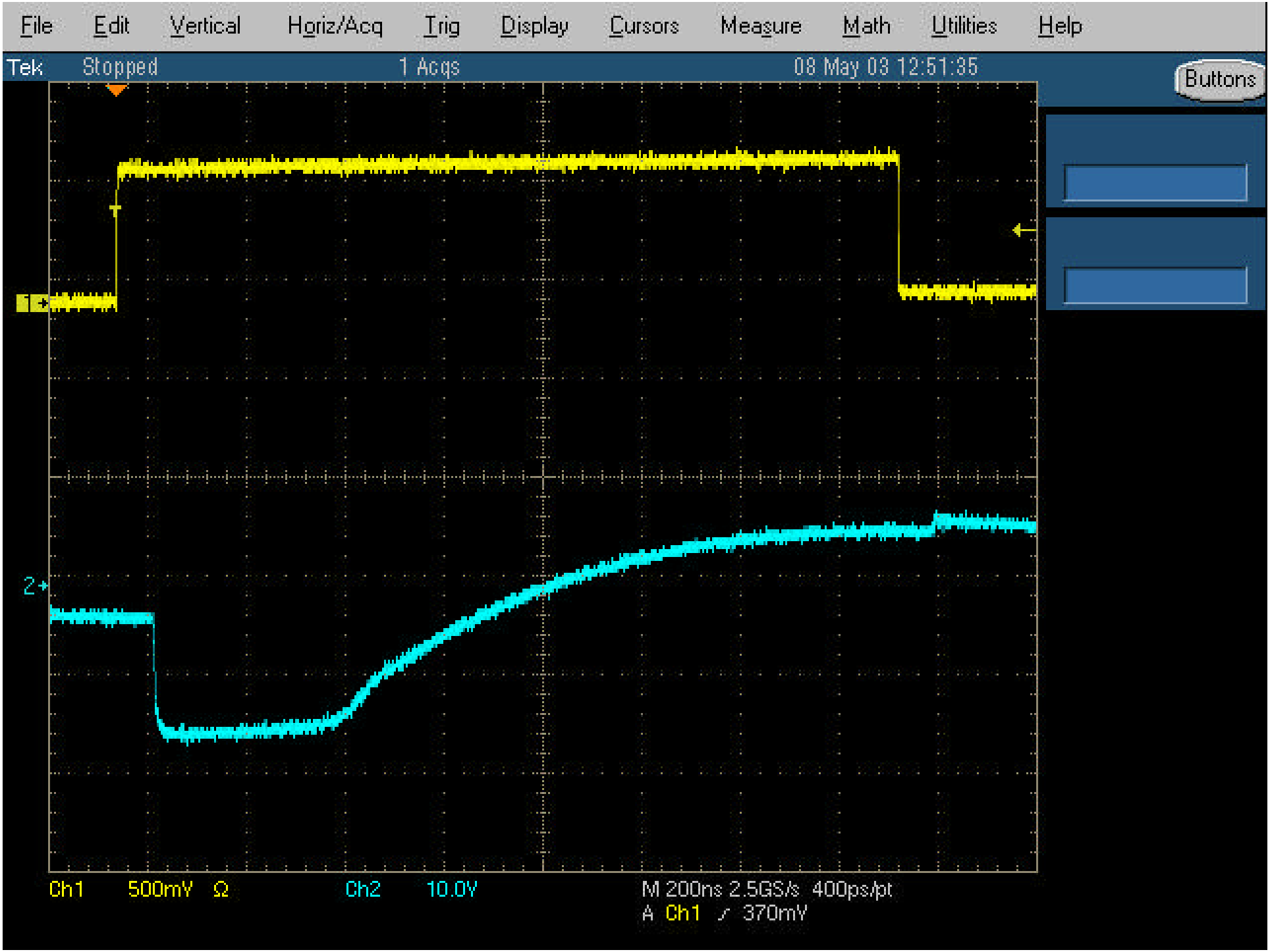
M 200ns 2.5GS/s 400ps/pt
A Ch1 ⟋ 370mV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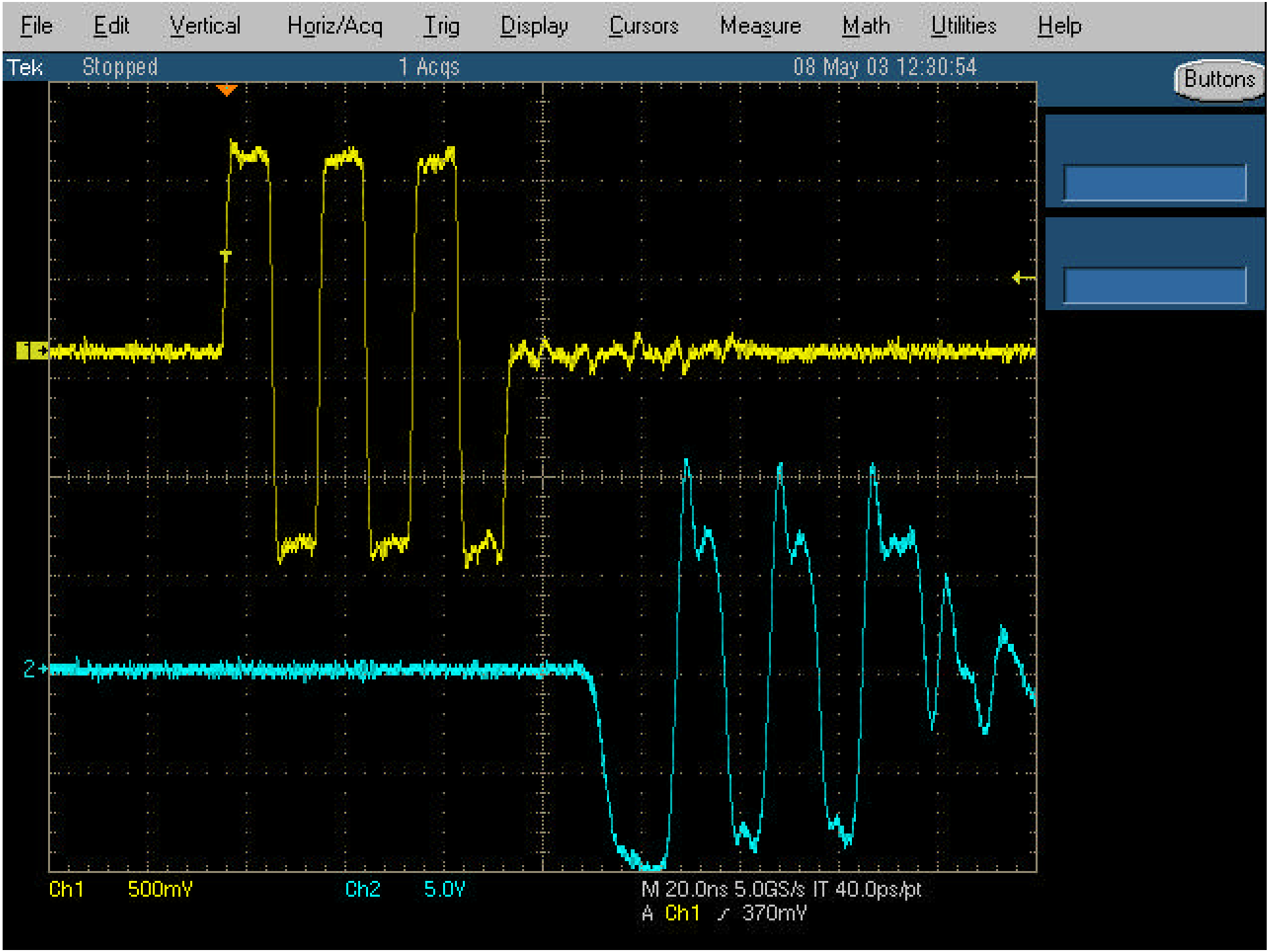
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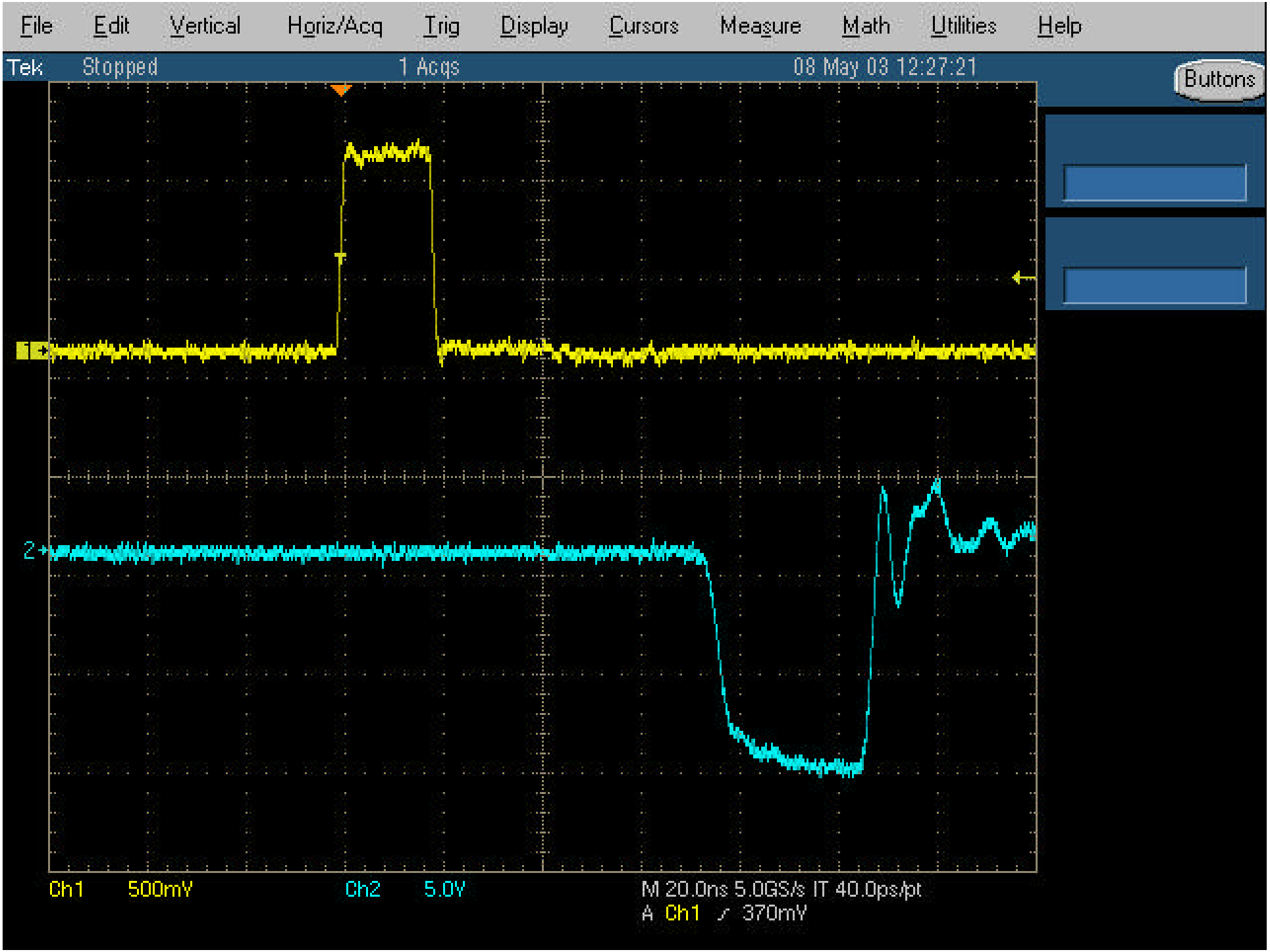
Ch2 5.0V
M 20.0ns 5.0GS/s IT 40.0ps/pt
A Ch1 ⟋ 370mV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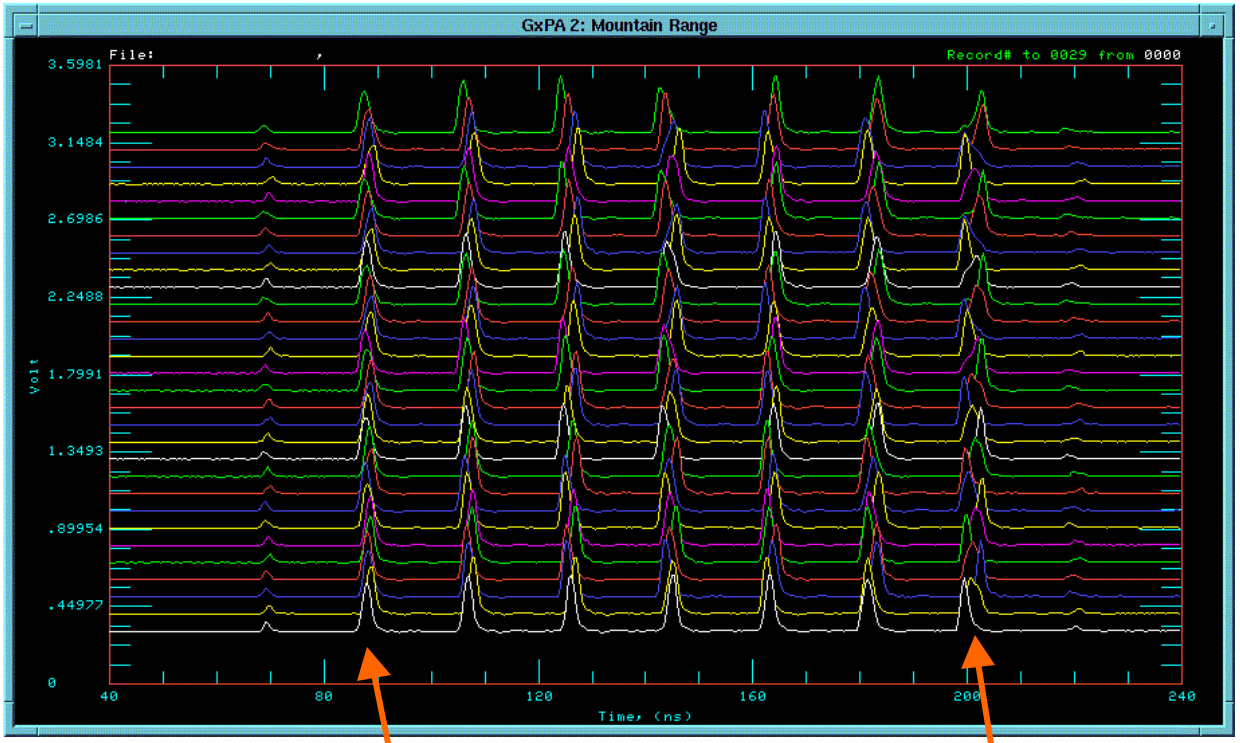
Ch2 5.0V
M 20.0ns 5.0GS/s IT 40.0ps/pt
A Ch1 ⟋ 370mV

Longitudinal Beam Instability in MI



- Occurs with as few as 7 bunches (out of 588)
- Prevents low emittance bunch coalescing and efficient Pbar bunch rotation

First Bunch ~ OK

7th Bunch Trashed

see Dave Wildman's Talk

- Driven by cavity wake fields within bunch train
- Seeded by Booster & amplified near MI flat top.

Longitudinal Damper Broadband RF Cavities
3 New Cavities, Similar to Recycler,
With Superior HF Response - (*Wildman)*

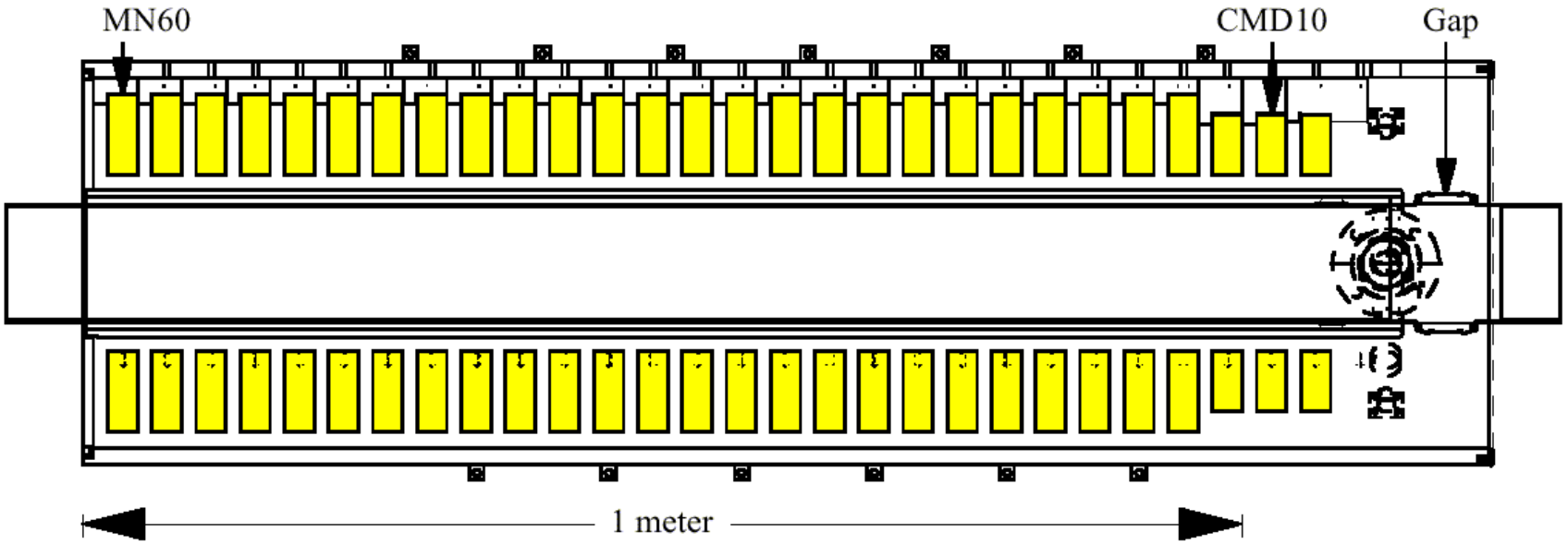
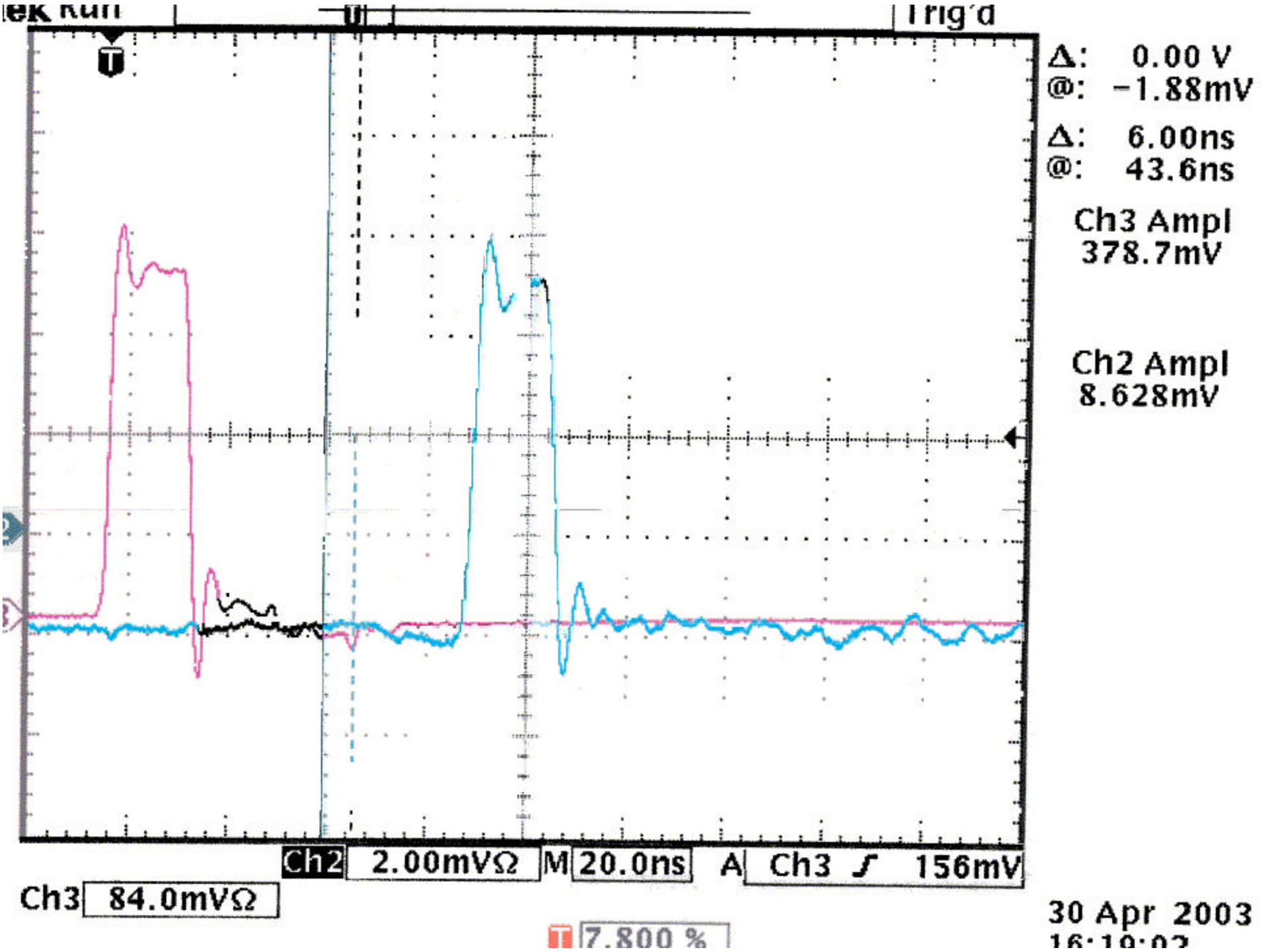


Figure 1: Schematic drawing of Recycler Wideband RF Cavity

Non-Resonant Cavity looks like 50-Ohm Load in parallel with a large Inductor


FRAGILE


Trig'd
Δ: 0.00 V
@: −1.88mV
Δ: 6.00ns
@: 43.6ns
Ch3 Ampl
378.7mV
Ch2 Ampl
8.628mV
Ch2 2.00mVΩ M 20.0ns A Ch3 ∫ 156mV
Ch3 84.0mVΩ
30 Apr 2003

Wideband Power Amplifiers

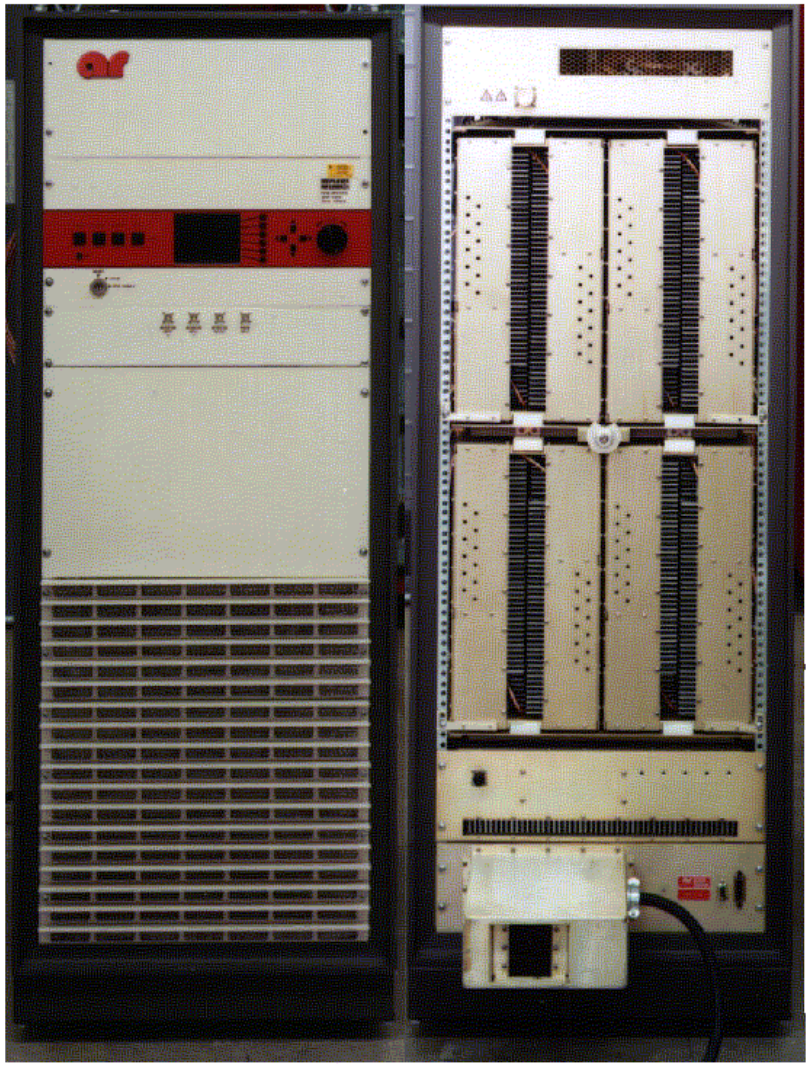


Figure 2: Front and Rear views of Amplifier Research model 3500A100.

- Recycler has four of these amps, capable of generating +/-2000V or arbitrary waveform.
- MI (D. Wildman) ordered 3 more for longitudinal Dampers, due May~June.
- Claim is still on schedule

✍ ~1800V of broadband voltage in MI

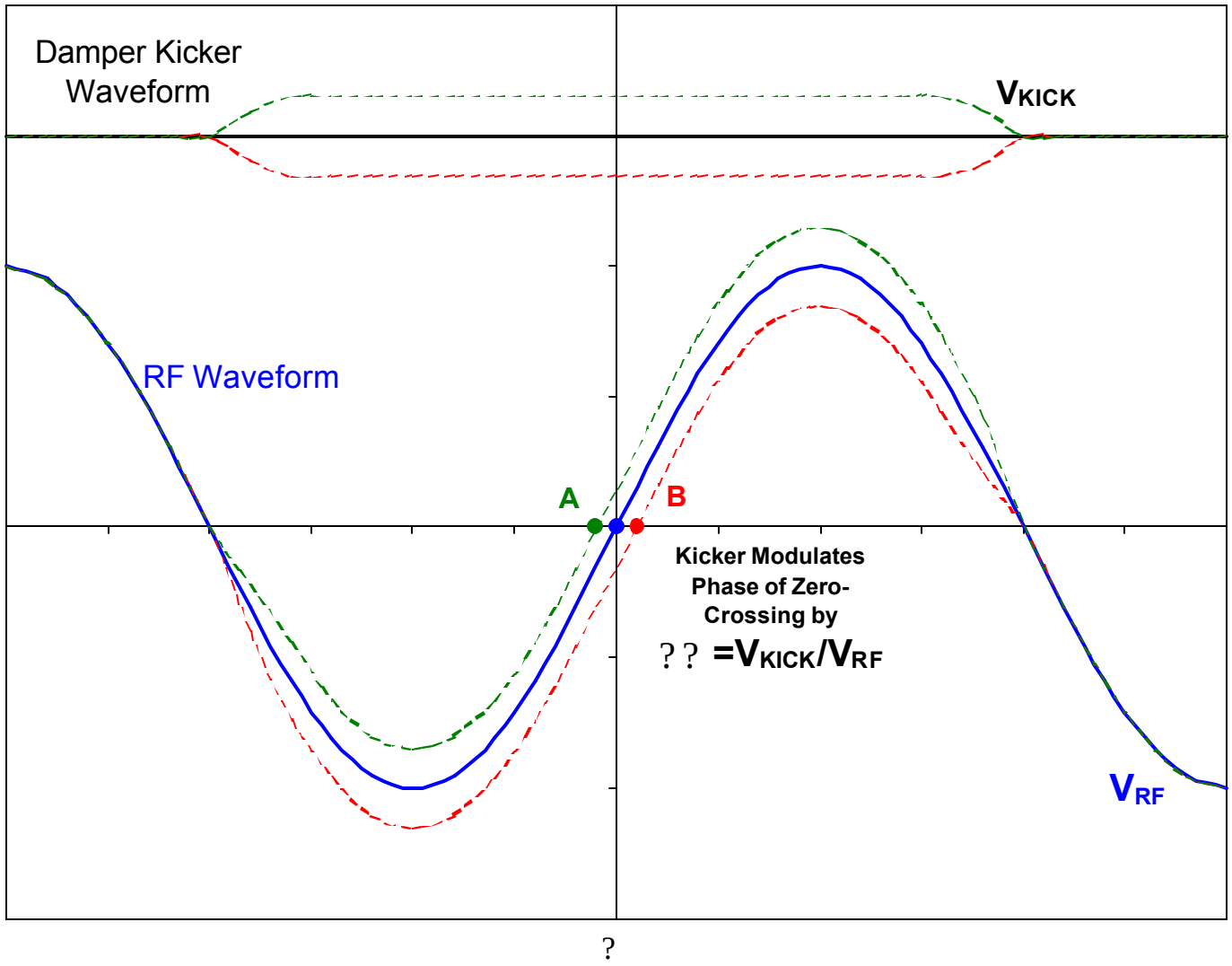
Pbars vs. Proton Timing: Longitudinal

- 3 Cavites spanning 5-10 meters
- Bunch-by-bunch kick needs separate fanout for Protons and Pbars
- Either:
  - One DAC per Cavity
  - Relay switch box with different cable delays ✍ *this option chosen* ✍ single TTL bit Pbar-P
  - Parts in (Dave Wildman's) hands

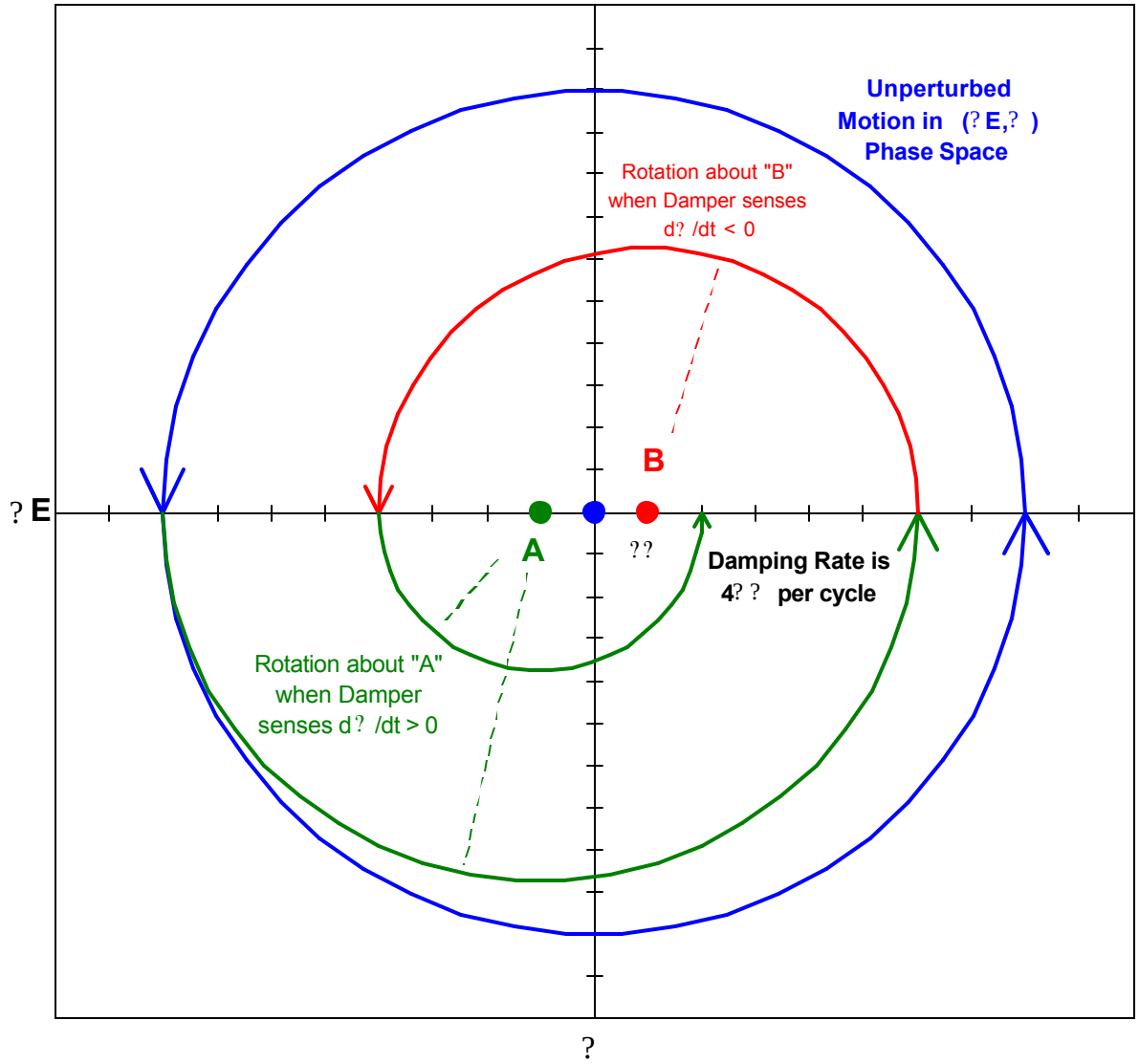
Longitudinal Damper in Main Injector

1. Benefits to Bunch Coalescing for Collider
   - "Dancing Bunches" degrade Proton coalescing and $?_L$
   - Affects Lum directly (hourglass) and indirectly (lifetime)
   - We are deliberately blowing $?_L$ in Booster
2. Benefits for Pbar Stacking Cycles
   - Bunch Rotation is generally turned off ! (x1.5 stack rate?)
   - Slip-Stacking etc. (Run IIb) will require stable bunches
3. Needed for eventual NUMI operation

Longitudinal Damper Works by Modulating Phase of RF Zero Crossing



Damping of Bunch Motion by Modulation of Center of Rotation (RF zero-crossing) on Alternate Half-cycles of Synchrotron Motion

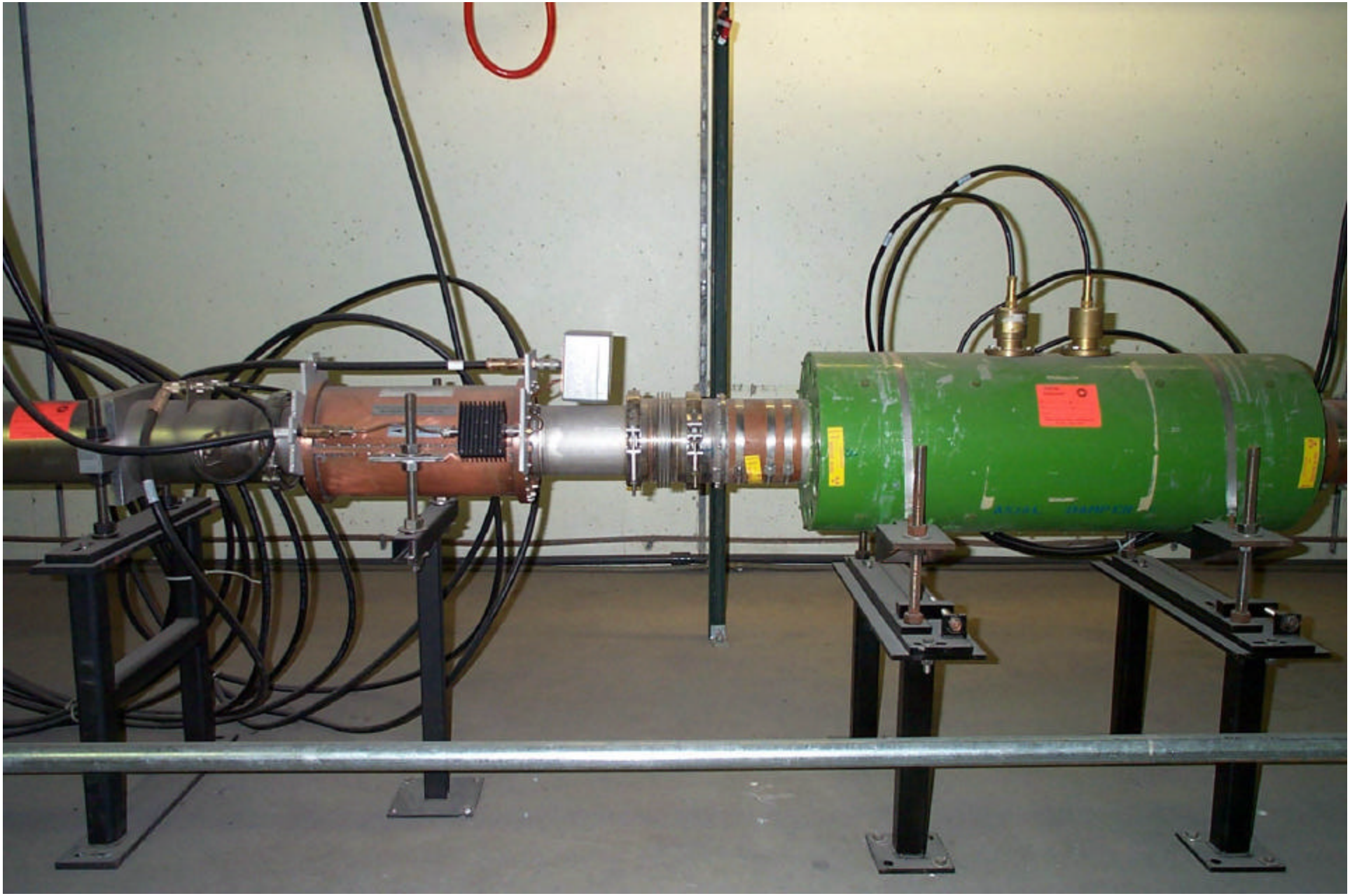


Numerical Examples for Longitudinal Dampers

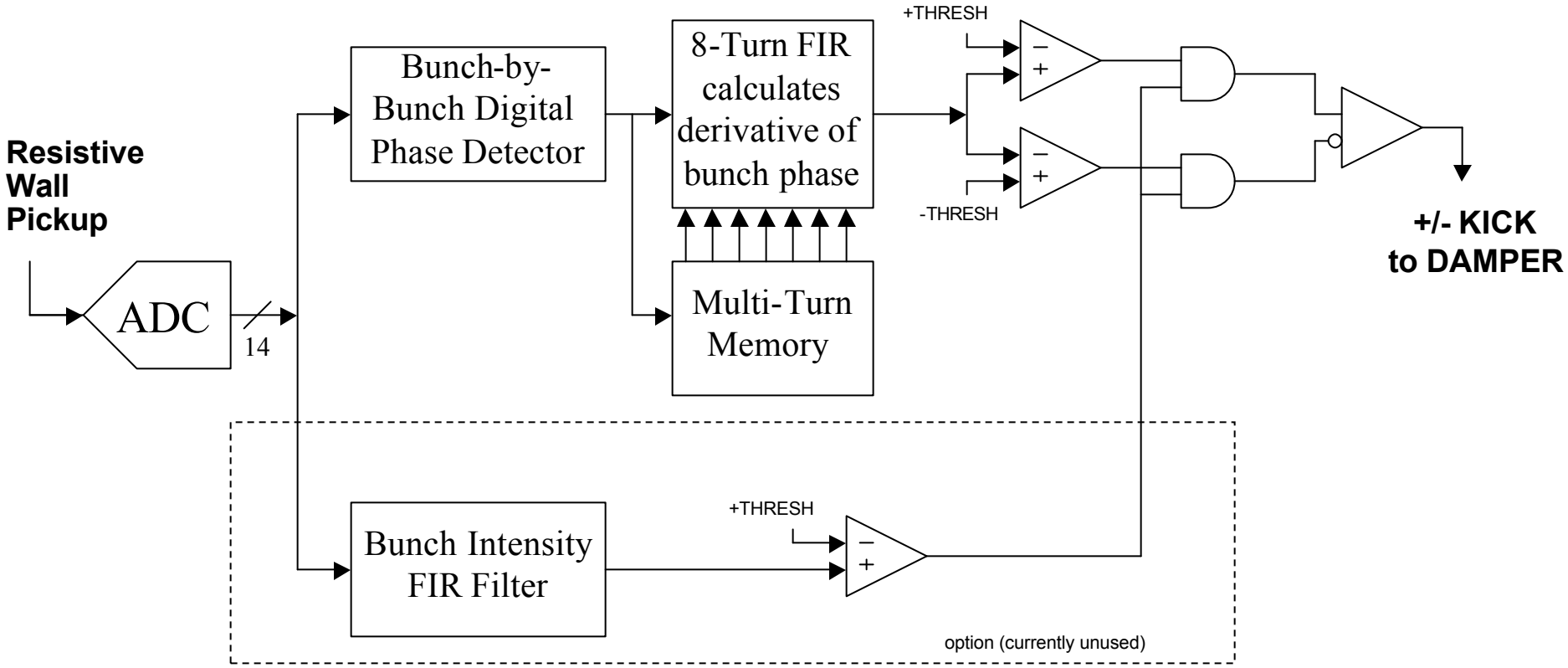
	MI at Injection	Recycler
RF Voltage	1000 kV	2 kV
Damper Voltage	0.6 kV	0.1 kV
RF frequency	53 MHz	2.5 MHz
Sychrotron Freq.	870 Hz	8.5 Hz
Damping Time for 20 degree phase osc.	145 periods	1.7 periods
	0.17 sec.	0.21 sec.

Damping can be made faster

by raising V_{DAMPER} and/or lowering V_{RF}



Longitudinal Damper FPGA Logic



Individual Bunches are kicked + or - depending on whether they are moving right or left in phase

FPGA Code for Universal Damper (8-turn Filter)

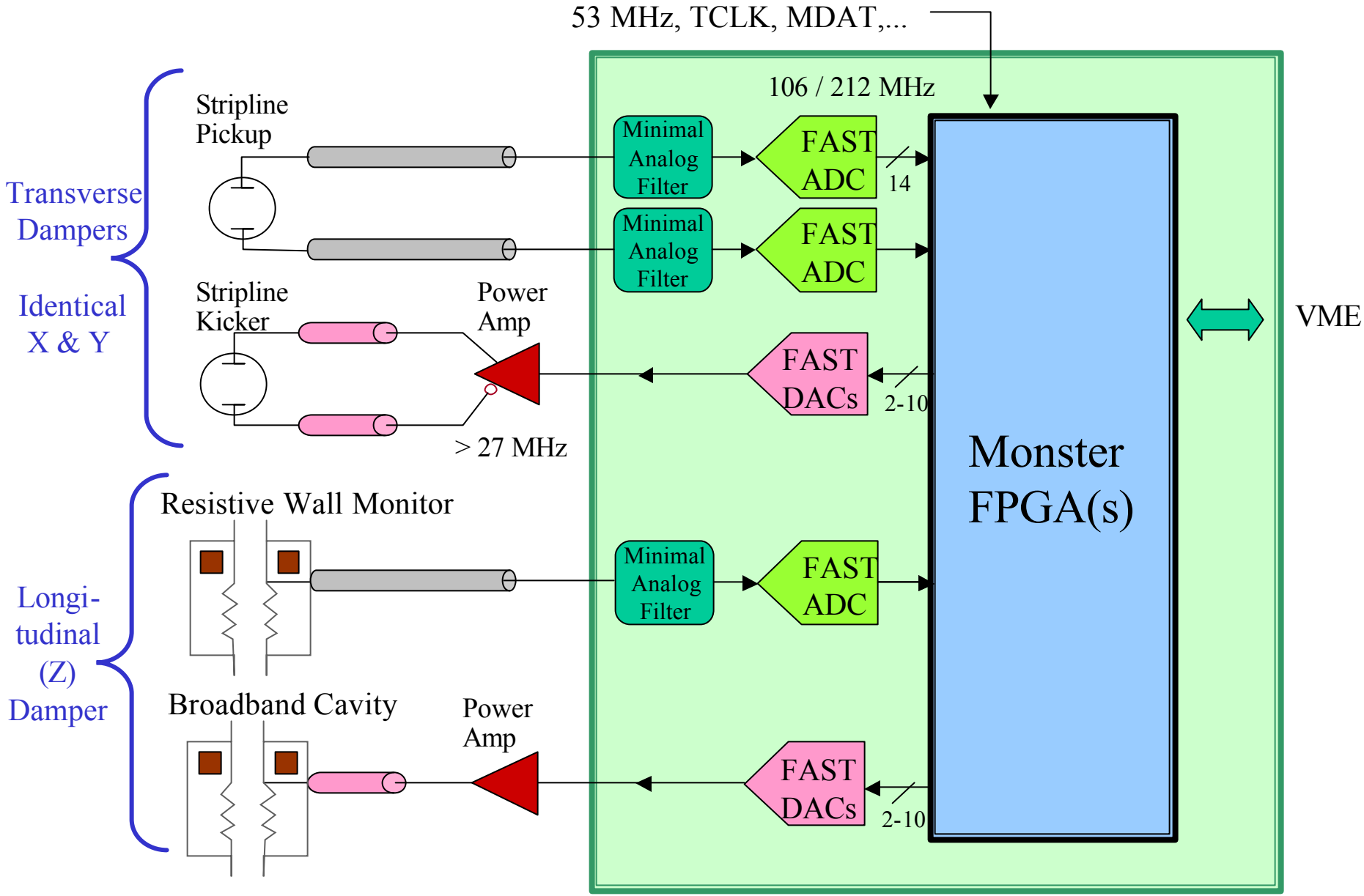
```
-- 7-Turn Delay Storage for 8-turn filter using altshift_taps megafunction (RAM-based shift register)
-------------------------------------------------------------------------------------------------
-- shift register length between taps is Main Injector/Recycler Harmonic number (588)
()= turn_delay : altshift_taps() with (NUMBER_OF_TAPS=7, WIDTH=15,
        TAP_DISTANCE=588) returns(.taps[0]);        -- # of stages between taps = # of bunches in ring
    turn_delay.clock = adc1kby2;                    -- megafunction 2-stage pipelined by 53 MHz clock
    turn_delay.shiftin[] = Qch1.q[14..0];           -- shiftreg input is Zero-turn delay signal

-- Multiply & Add pipelined megafunctions to get 8-turn weighted sum for FIR filter
-------------------------------------------------------------------------------------
-- Four multipliers and adders in each pipelined megafunction, two megafunctions for 8 total multipliers
-- first multiplier/adder for turns n,n-1,n-2,n-3
()= Mpy_Add :   altmult_add()       with (NUMBER_OF_MULTIPLIERS=4, WIDTH_A=15, WIDTH_B=4, WIDTH_RESULT=21,
                                          REPRESENTATION_A="SIGNED",REPRESENTATION_B="SIGNED",
                                          INPUT_REGISTER_A0="CLOCK0",INPUT_REGISTER_A1="CLOCK0",
                                          INPUT_REGISTER_A2="CLOCK0",INPUT_REGISTER_A3="CLOCK0",
                                          INPUT_REGISTER_B0="CLOCK0",INPUT_REGISTER_B1="CLOCK0",
                                          INPUT_REGISTER_B2="CLOCK0",INPUT_REGISTER_B3="CLOCK0")
                                    returns(.result[0]);    -- 1-bit dummy, actually returns nothing
    Mpy_Add.datab[15..0]    = FIR_coeffs[15..0];        -- multiply by four 4-bit signed numbers from VME control registers
    Mpy_Add.dataa[14..0]    = Qch1.q[14..0];            -- zero turn delay is multiplier port A0
    Mpy_Add.dataa[59..15]   = turn_delay.taps[44..0];   -- 1,2, and 3 turn delays are multiplier ports A1,A2,A3
    Mpy_Add.clock0  = adc1kby2;                         -- pipelined result comes out 3 clocks later

-- second multiplier/adder for turns n-4,n-5,n-6,n-7
()= Mpy_Add2    :   altmult_add()       with (NUMBER_OF_MULTIPLIERS=4, WIDTH_A=15, WIDTH_B=4, WIDTH_RESULT=21,
                                          REPRESENTATION_A="SIGNED",REPRESENTATION_B="SIGNED",
                                          INPUT_REGISTER_A0="CLOCK0",INPUT_REGISTER_A1="CLOCK0",
                                          INPUT_REGISTER_A2="CLOCK0",INPUT_REGISTER_A3="CLOCK0",
                                          INPUT_REGISTER_B0="CLOCK0",INPUT_REGISTER_B1="CLOCK0",
                                          INPUT_REGISTER_B2="CLOCK0",INPUT_REGISTER_B3="CLOCK0")
                                    returns(.result[0]);    -- 1-bit dummy, actually returns nothing
    Mpy_Add2.datab[15..0]   = FIR_coeffs[31..16];       -- multiply by four 4-bit signed numbers from VME control registers
    Mpy_Add2.dataa[59..0]   = turn_delay.taps[104..45]; -- 4,5,6, and 7 turn delays are multiplier ports A0,A1,A2,A3
    Mpy_Add2.clock0 = adc1kby2;                         -- pipelined result comes out 3 clocks later

-- Add Damper results of both Multiply/Add megafunctions to get final result for 8-turn weighted sum
()= mpySum  : lpm_add_sub() with (lpm_width=22, lpm_direction="add") returns (.cout);
    mpySum.dataa[20..0]     = mpy_add.result[20..0];        -- add result of first four multipliers
    mpySum.dataa[21]        = mpy_add.result[20];           --      (sign extend)
    mpySum.datab[20..0]     = mpy_add2.result[20..0];       -- add result of second four multipliers
    mpySum.datab[21]        = mpy_add2.result[20];          --      (sign extend)
-- Output Register for calculated kick sum
()= DK: lpm_ff (.data[] = mpySum.result[], .clock = adc1kby2) with (lpm_width=22) returns (.q[0]);
```

All-Coordinate Digital Damper



Digital Signal Processing with FPGA's

- Commercial card from Echotek
  - 8 channels of 14-bit, 106 MHz Digitization
- One card does all dampers for one machine
- Customized FPGA firmware
  - Bill Ashmanskas
  - GW Foster
  - Warren Schappert…
- Handles Wide Variety of Bunch Structure

"Universal-Damper" Application: Signal Processing Steps (transverse)

Echotek Board

1) Bandwidth-Limit input signal to ~53 MHz
2) 14 Bit Digitization at 106 MHz or 212 MHz

Inside FPGA

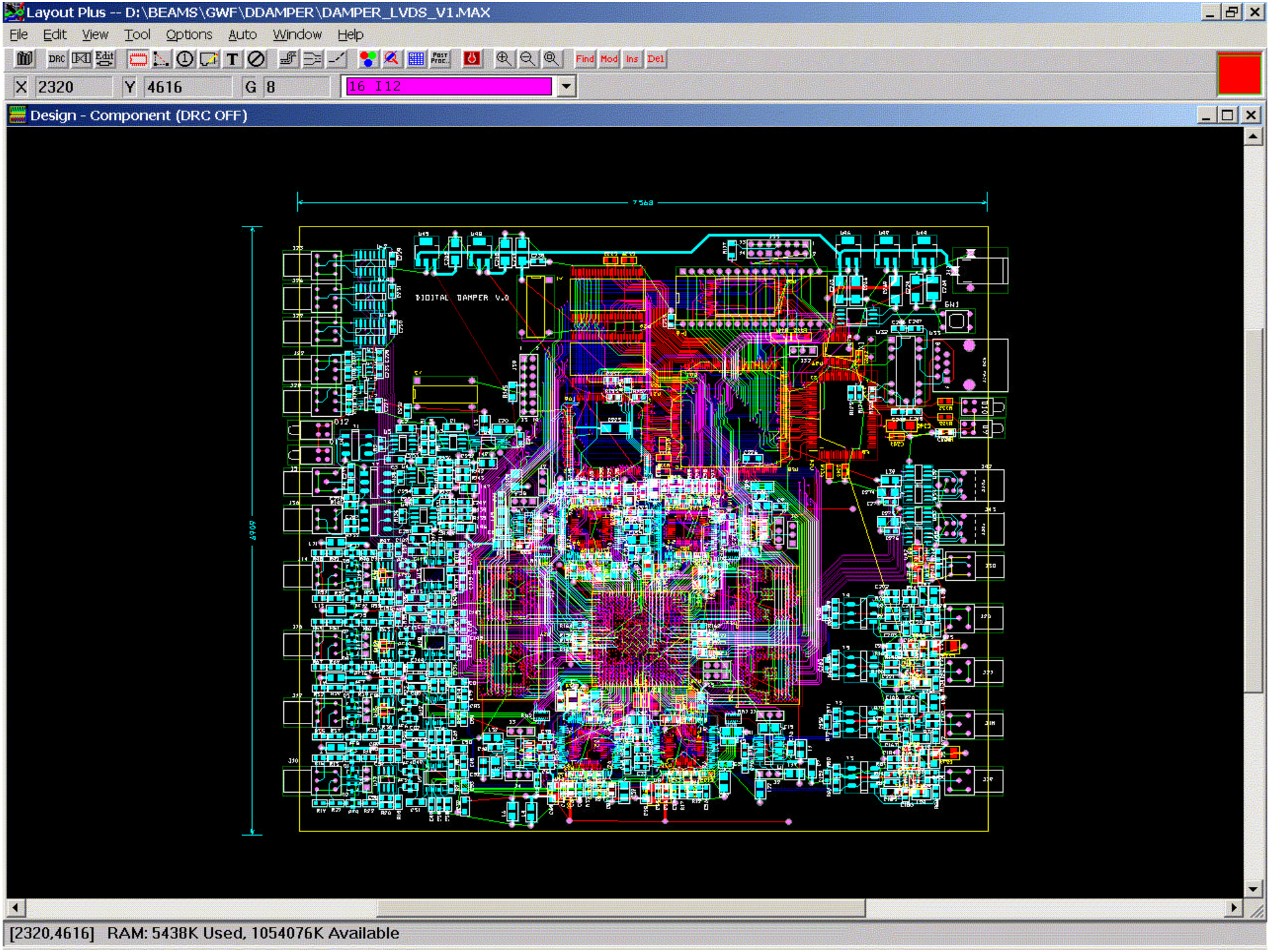
3) FIR filter to get single-bunch signal
4) Sum & Difference of plate signals
5) Multi turn difference filter (FIR) w/delay
6) Pickup Mixing for correct Betatron Phase
7) Bunch-by-bunch gain, dead band etc.
8) Timing Corrections for Frequency Sweep
9) Pre-Distortion for Kicker Power Amp

Buy

10) Power Amp for Kicker

New Damper Board (A. Seminov)

- *SINGLE* high-end FPGA (vs. 5 on Echotek)
- Four 212 MHz ADCs (vs. 106 MHz on Echotek)
- Four 424 MHz DACs (vs. 212 MHz on Echotek)
- Digital Inputs:
  - TCLK, MDAT, BSYNCH, 53 MHz, Marker
- Digital Outputs:
  - Pbar/P TTL, scope trigger, 1 GHz serial Links..
- "NIM module" with Ethernet interface to ACNET


Layout Plus -- D:\BEAMS\GWF\DDAMPER\DAMPER_LVDS_V1.MAX
File Edit View Tool Options Auto Window Help
X 2320 Y 4616 G 8
16 I12
Design - Component (DRC OFF)
DIGITAL DAMPER V.0
[2320,4616] RAM: 5438K Used, 1054076K Available

Adding a new ACNET Device

1) Add register(s) to FPGA Firmware

```
-- TEST DEVICE     -- captures Damper Filter output for bucket #23 for Fast-Time Plot

IF (dsel.q & addr[]==H"0088") THEN          -- VME Address decode
    datatri[]= lpm_ff(                      -- connect register to VME read data bus
        .clock  =   adclkby2,               -- clocked at 53 MHz
        .enable =   Bucket_Count==23,       -- clock enabled when RF bucket counter=23
        .data[] =   Filter_Out_32_bit[])    -- data from filter output
        with (LPM_WIDTH=32);                -- register is 32 bits wide
END IF
```

2) Start Recompile (takes ~6 minutes)

3) Meanwhile, use DABBEL/D80 to define properties of new ACNET device

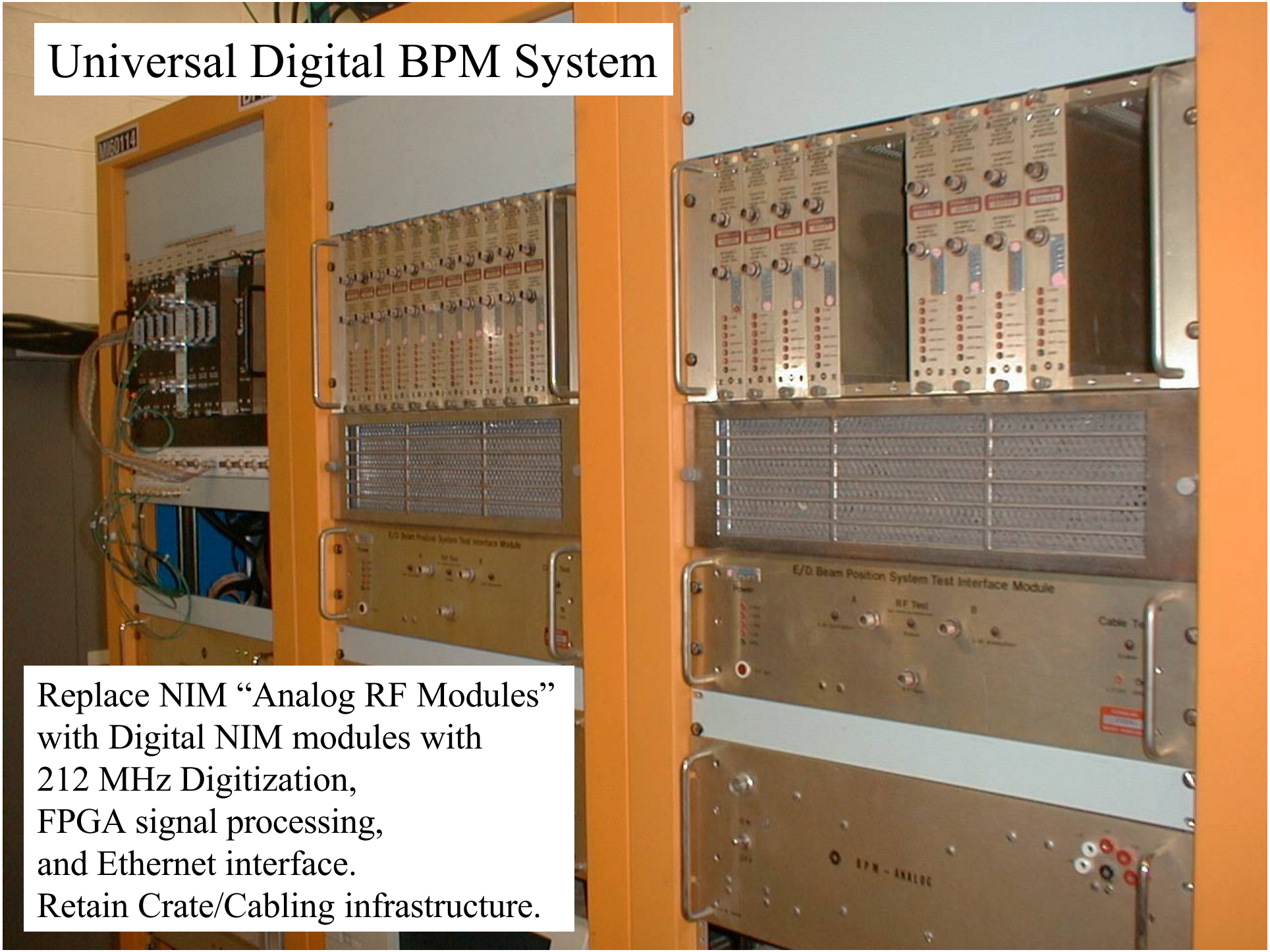
4) Download Firmware & Reboot Crate (~2 min.)

✍ *Takes about 10 minutes from concept to Fast-Time Plot*

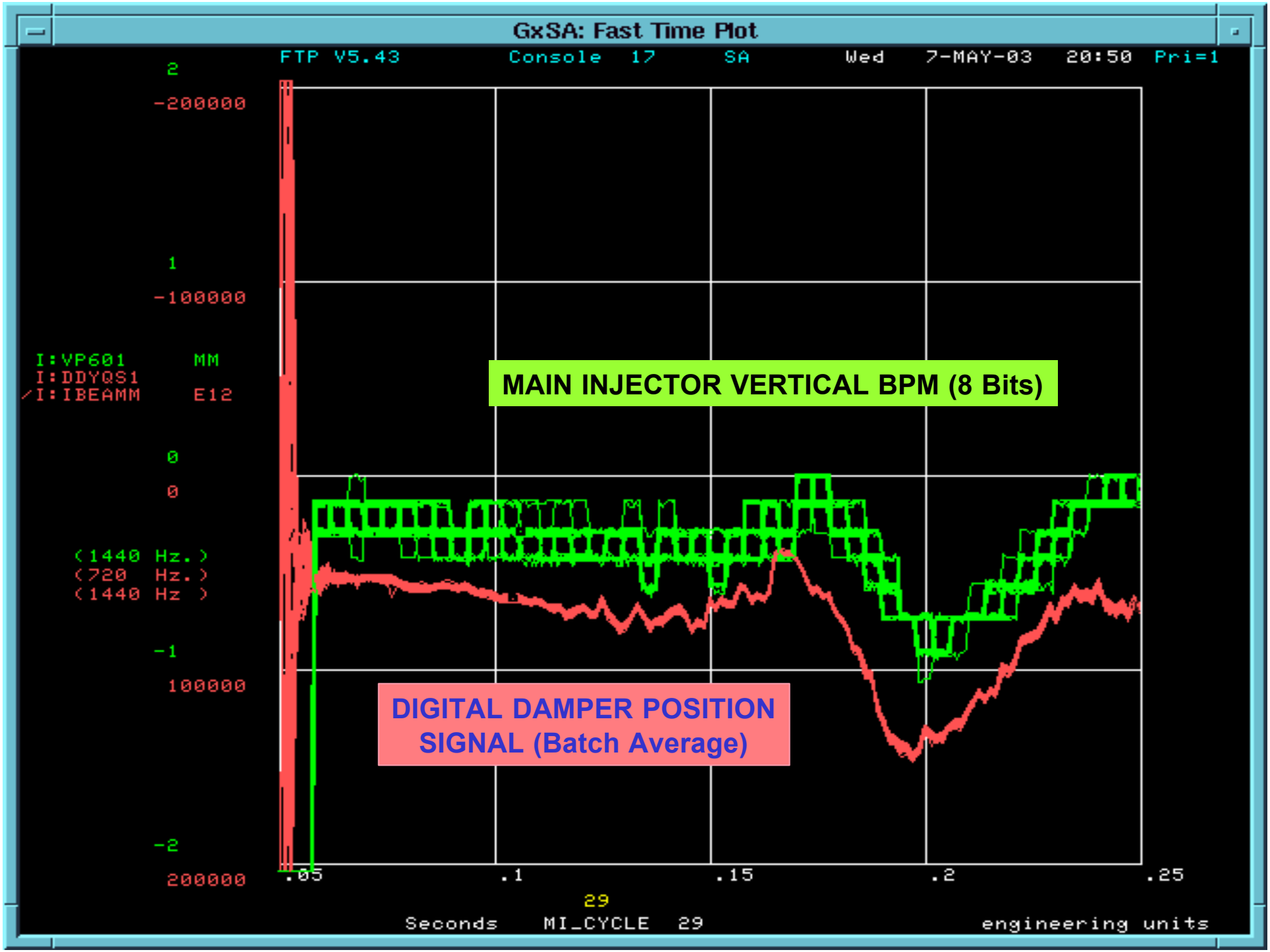
Other Applications of this Digital/FPGA Hardware Approach

- Universal BPM System
- Generic Instrumentation with shared Hardware/Software infrastructure
- God's Own Beam Loading Compensation
- Replacing Booster LLRF with one "Digital NIM" module

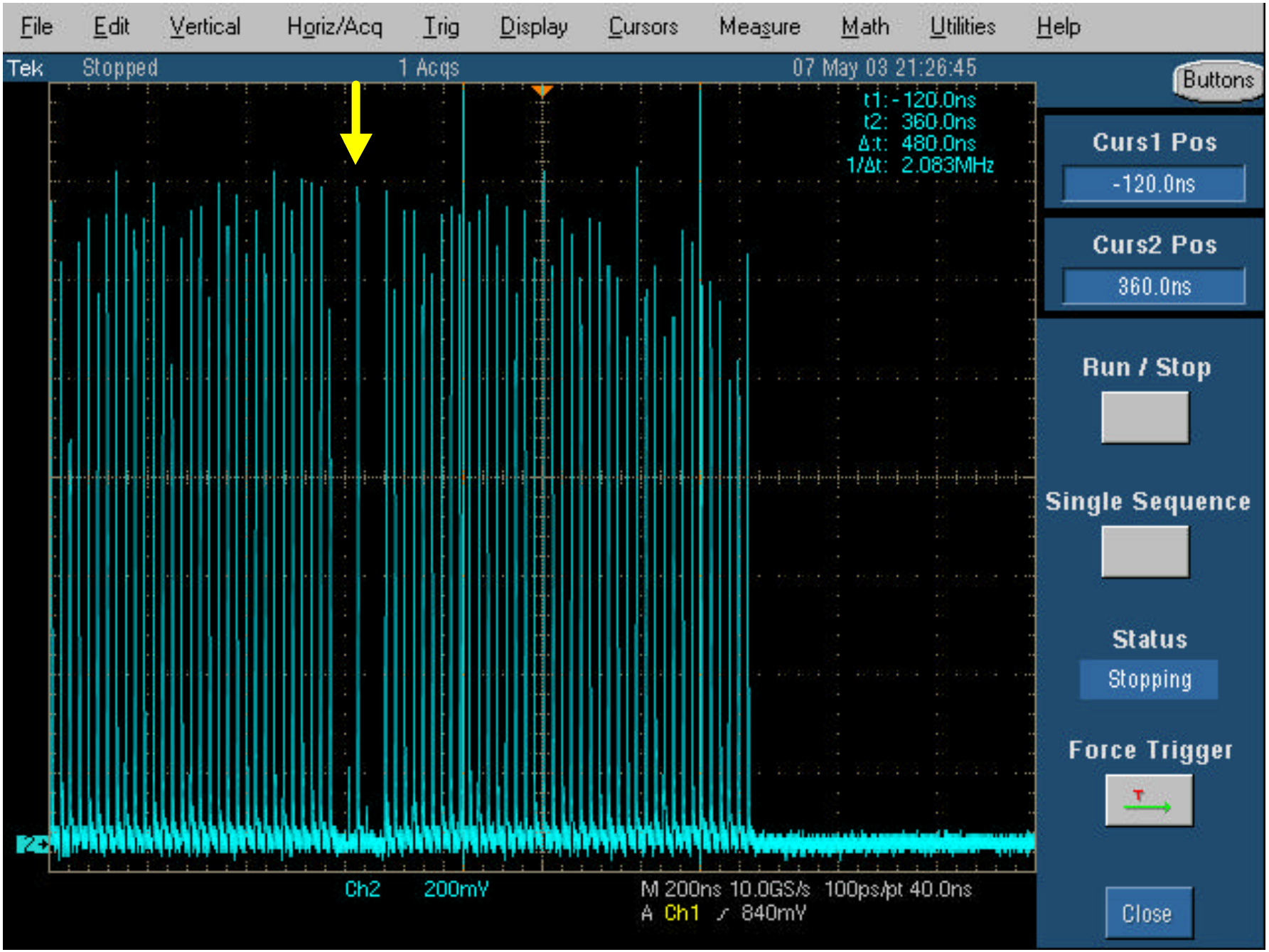
Universal Digital BPM System

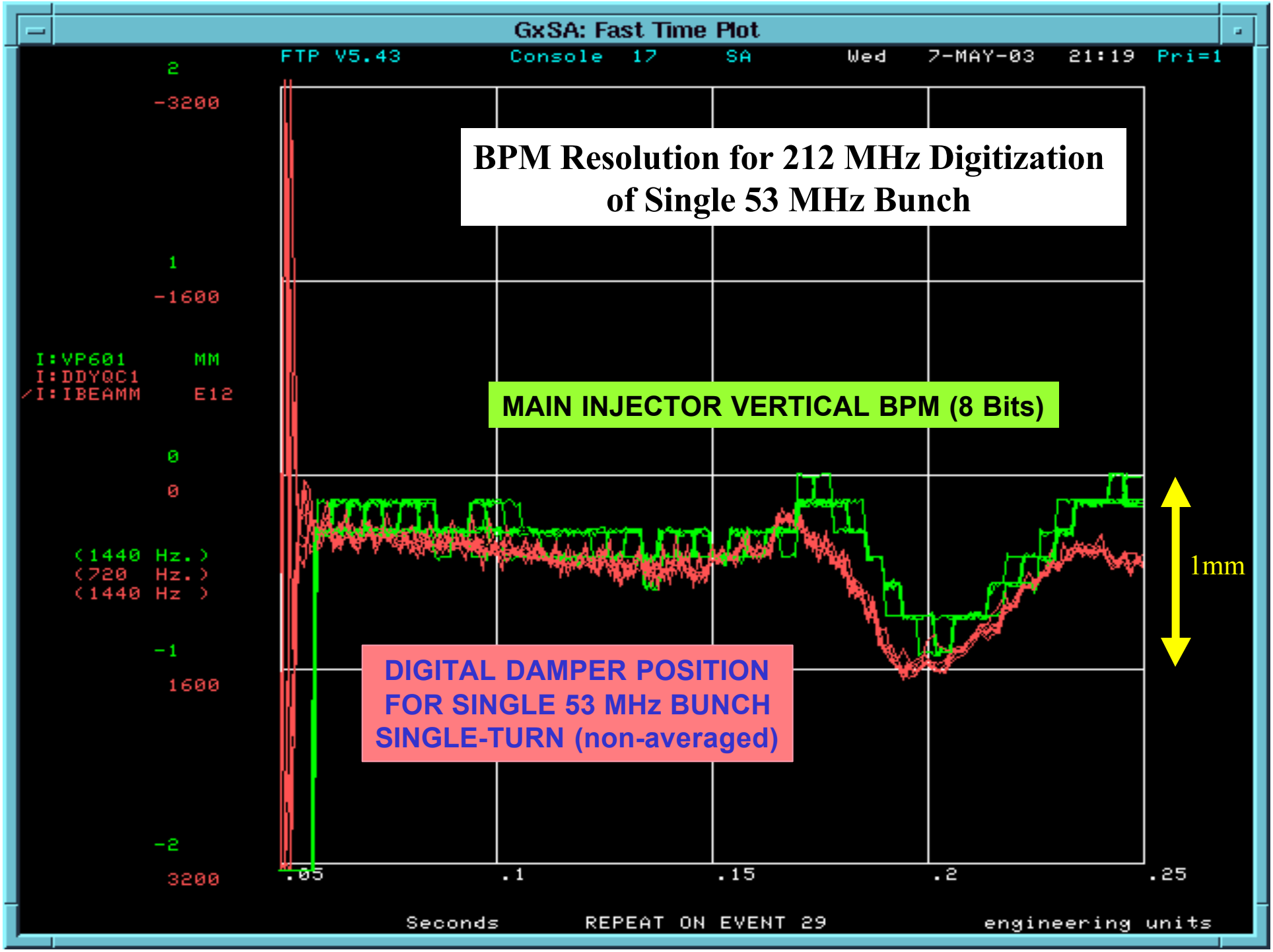


Replace NIM “Analog RF Modules”
with Digital NIM modules with
212 MHz Digitization,
FPGA signal processing,
and Ethernet interface.
Retain Crate/Cabling infrastructure.


GxSA: Fast Time Plot
FTP V5.43
Console 17
SA
Wed 7-MAY-03 20:50 Pri=1
2
-200000
1
-100000
I:VP601 MM
I:DDYQS1
/I:IBEAMM E12
0
0
(1440 Hz.)
(720 Hz.)
(1440 Hz)
-1
100000
-2
200000
MAIN INJECTOR VERTICAL BPM (8 Bits)
DIGITAL DAMPER POSITION SIGNAL (Batch Average)
.05
.1
.15
.2
.25
29
Seconds
MI_CYCLE 29
engineering units

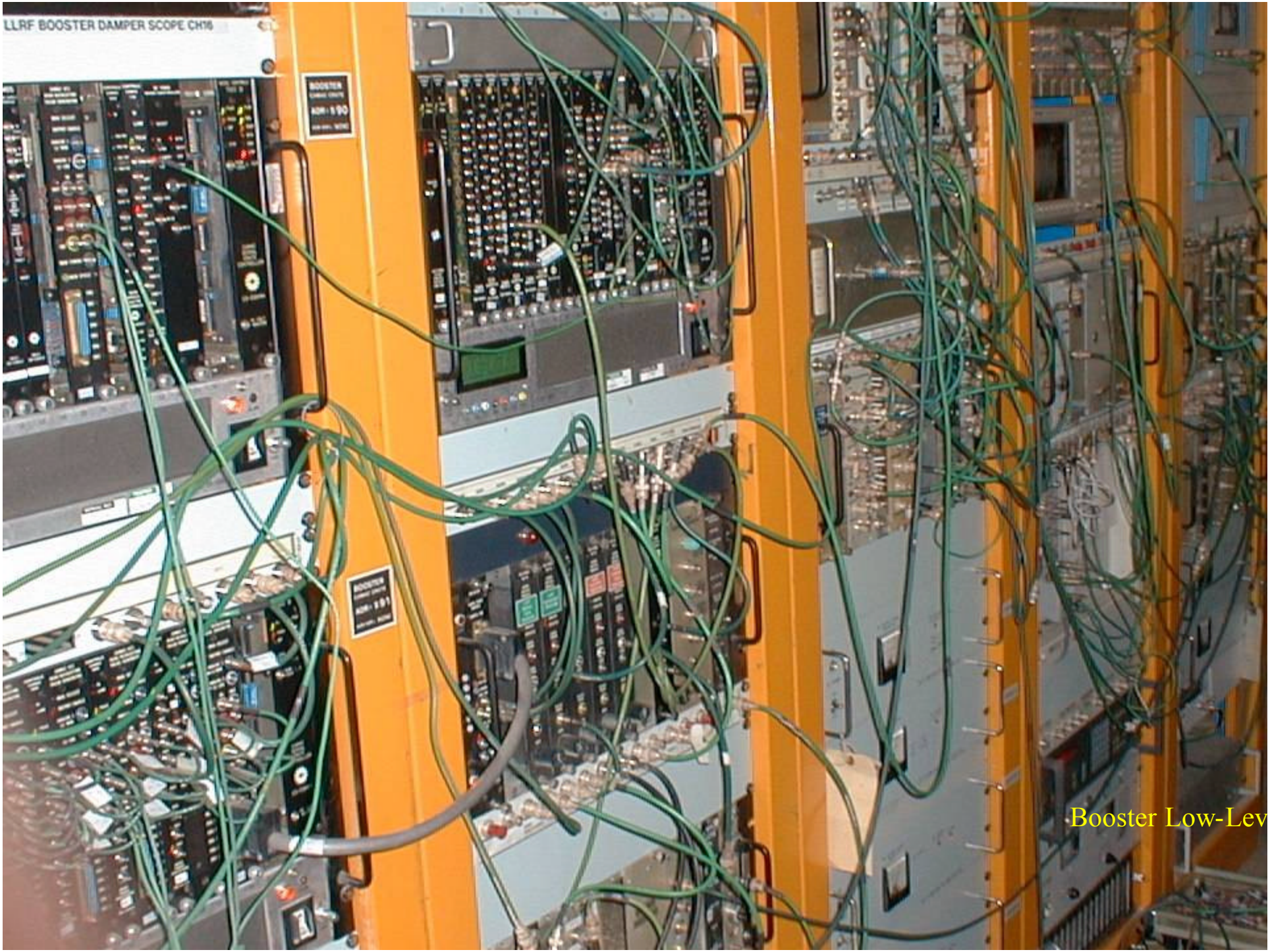
Single-Bunch BPM Measurement was tested by blowing out nearby bunches during Stacking Cycle




GxSA: Fast Time Plot
FTP V5.43 Console 17 SA Wed 7-MAY-03 21:19 Pri=1
2
-3200
1
-1600
I:VP601 MM
I:DDYQC1
/I:IBEAMM E12
0
0
(1440 Hz.)
(720 Hz.)
(1440 Hz)
-1
1600
-2
3200
.05
.1
.15
.2
.25
Seconds
REPEAT ON EVENT 29
engineering units
BPM Resolution for 212 MHz Digitization of Single 53 MHz Bunch
MAIN INJECTOR VERTICAL BPM (8 Bits)
1mm
DIGITAL DAMPER POSITION FOR SINGLE 53 MHz BUNCH SINGLE-TURN (non-averaged)

Booster Low-Level RF.

The Final Frontier.


LLRF BOOSTER DAMPER SCOPE CH16
Booster Low-Lev